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Avalanche mode operation of transistors

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AVALANCHE MODE OPERATION
OF TRANSISTORS

by

Raymond Arthur Kjar

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ABSTRACT

The fact that avalanche multiplication in a transistor can be used to provide regenerative feedback has been known for some time. Circuits utilizing this effect have been used to obtain very high switching speeds. Essentially all methods of analysis of such circuits have been based upon models developed for germanium alloy junction transistors.

The experiments in this study were performed with silicon planar transistors. It was found that the performance of a transistor in the avalanche mode is greatly influenced by transverse voltages in the base region. The base currents during switching lead to a considerable pinch-in of the current carrying area of the transistor, and the distribution of the collector capacitance emphasizes this effect. A model for the avalanche transistor is developed which includes the changes resulting from pinch-in and is superior to previous models used for the analysis of avalanche switching. The necessary modifications to the previous model include a base spreading resistance through which most of the collector to base capacitance of the transistor must be coupled. If the pinch-in is severe, this resistance can become quite high and nearly isolate the capacitive feedback from the active area of the transistor.

It is shown that transistors with collector breakdown voltages of 10 to 20 volts are potentially superior for avalanche operation. Operation with any lower breakdown voltage is found to be impractical because of the threshold effect in avalanche multiplication. This, rather than internal field emission, proves to be the important limitation upon

low voltage operation.

Finally some simple pulse circuits were constructed to demonstrate applications of base turn-off control. One of these circuits, when used with a low voltage transistor, produced 2 nsec. pulses and had an 8 nsec. recovery time.

INTRODUCTION

It has been known for some time that avalanche multiplication in the collector of a transistor permits its use as a bistable switch (1). The effect of avalanche is to produce a common base current gain greater than 1, and the resulting characteristics are similar to those of a PNPN controlled switch. The advantage of the avalanche transistor over the PNPN device lies in its ability to switch into the conducting state very fast. Collector voltage rise times of less than a nanosecond are easily achieved. Perhaps the major application of avalanche transistors is in the generation of pulses with very fast rise times. Such a method is used to generate the sampling pulse in a commercial sampling oscilloscope, and it is this oscilloscope which was used to obtain the measurements for this study.

Statement of Problem

A major difficulty in the use of an avalanche transistor as a bistable switch is the relatively high collector voltage which exists while the transistor is in the conducting state. This may easily be one half of the collector breakdown voltage or better. Not only does this limit the useful range of collector voltage, but a large part of the power is dissipated in the transistor rather than the collector load resistance, and this severely limits the power handling capability of the transistor. A major objective of this study is to show what can be done in the construction of the transistor to achieve significant avalanche multiplication at lower collector voltages in comparison to

the breakdown voltage. This will result in more of the supply voltage appearing across the load resistance and less across the transistor.

The turn-off time of any transistor is limited by the time constant of the collector circuit including the internal collector capacitance of the transistor. The tendency has been to use transistors with high breakdown voltages for avalanche operation. Operation at lower voltages and with the same currents reduces the collector time constant, and should permit faster turn-off times. If the operation at lower voltages is to be avalanche operation it is necessary to use transistors with lower breakdown voltages. The question arises as to how low of a breakdown voltage can be obtained in the collector junction while still retaining the properties desired for avalanche mode operation. This is one of the questions to be answered in this study.

Any detailed analysis of avalanche mode operation of transistors to date deals specifically with the properties of alloy junction germanium transistors. The final objective is to note any differences in the operation of more modern types of transistors as compared to those previously analyzed. The double diffused structure is becoming standard, and an immediate question is how previous models of avalanche transistors can be adapted to this type of transistor. Of particular interest is an analysis of turn-off as this has not been studied in detail.

Contribution to Solution

First a study of the avalanche multiplication ratios of various junctions was undertaken. Information already available dictated the

use of NPN silicon transistors for avalanche mode operation. It was found that the collector junction should be a step junction if the collector voltage during conduction is to be minimized for a given collector breakdown voltage. Furthermore it was shown that there is an optimum collector breakdown voltage of about 15 volts, which results in the largest possible portion of the collector voltage range being used in a bistable operation.

There is a threshold effect in avalanche multiplication which is instrumental in determining the optimum collector breakdown voltage. This threshold effect limits the minimum collector voltage during conduction to a high enough value that on this basis alone collector breakdown voltages of much less than 10 volts become impractical. It is this threshold effect rather than the onset of Zener breakdown from internal field emission which is most important in preventing operation of avalanche transistors at extremely low voltages.

Measurements of the switching transients of silicon planar transistors revealed that there is a considerable effect due to transverse currents in the base during switching. This effect was not considered in previous studies of avalanche transistors. At least for the type of transistors used in this study, however, there is a considerable pinch-in of the area actually carrying current as a result of the fields set up by these transverse currents. An analysis of the factors which influence this pinch-in effect is made.

Also considerable attention is given to the use of base control to turn off a transistor operating in the avalanche mode. This method

results in a much faster turn-off than any other approach, but may lead to considerable complications at high current levels. Two circuits are constructed to show possible applications of this method of turn-off. The first of these is a monostable circuit in which part of the output is delayed and used to turn the transistor off again. The second is a generator of short, fast rise, pulses similar to that commonly used with avalanche transistors. The difference is that a turn-off pulse is generated in addition to the output pulse and this is used to reset the transistor and alleviate the recovery time problems which such circuits generally have.

BACKGROUND

Secondary Ionization

Initially breakdown in semiconductor junctions was thought to be due to internal field emission. Later McKay and McAfee (2) showed that in most junctions breakdown is due to secondary ionization which results when minority carriers enter the reverse biased junction. Because of the similarity to breakdown in gases this has been named avalanche breakdown.

Of particular importance in transistors is the effect of secondary ionization at voltages which are less than the breakdown voltage. Suppose a number of electrons, n_1 , enters a reverse biased PN junction from the P side. The junction is a region of high electric field, and these electrons will be accelerated to velocities of around 10^7 cm./sec. They then have enough energy to create hole-electron pairs through collisions with valence electrons. The carriers thus generated may also become very energetic and result in more ionizing collisions. The end result is that an increased number of electrons, n_2 , reach the N side of the junction. These electrons are said to have been multiplied by the avalanche multiplication factor for electrons, M_n , which is defined as

$$M_n = n_2/n_1. \quad (1)$$

There is a corresponding multiplication factor, M_p , for holes entering from the N side of the junction, and there is also such a factor, M_i , for hole-electron pairs generated thermally within the junction (3) (4).

In general all three are different at junction voltages less than the breakdown voltage.

All of these multiplication factors increase with an increase in the reverse voltage applied to the junction, and at the avalanche breakdown voltage they approach infinity. Avalanche multiplication and even breakdown are in themselves non-destructive. As long as power dissipation is not so great as to cause excessive heating, the junction will not be damaged. In a diode the important effect of avalanche multiplication is to limit the reverse voltage which can be applied to the junction. At voltages below breakdown its only effect is to increase the reverse leakage current. In contrast, avalanche multiplication completely changes the characteristics of a transistor over a wide range of collector voltage.

The Avalanche Transistor as a Bistable Switch

Effects of Avalanche Multiplication

The common base current gain of a transistor, h_{FB} , is the product of an emitter efficiency, γ , a transport factor, β , and a collector efficiency, α^* . Except for collector voltages near saturation, α^* is simply the avalanche multiplication factor of the collector junction for minority carriers entering from the base region. For an NPN transistor

$$h_{FB} = \gamma \beta M_n \quad (2)$$

and

$$I_C = I_{CBO} + h_{FB} I_E \quad (3)$$

From these equations it might appear that quite large values of M_n will not prevent common base operation of a transistor. In actuality large values of M_n can lead to a negative input impedance which results in instability, and transistors in the common base configuration are seldom used near the collector breakdown voltage.

In the more often used common emitter configuration collector multiplication serves as a positive feedback, and even fairly low values of multiplication can have a great effect. The common emitter current gain is related to the common base current gain by

$$h_{FE} = \frac{h_{FB}}{1 - h_{FB}} \quad (4)$$

and in this configuration

$$I_C = I_{CBO} + h_{FE}(I_{CBO} + I_B). \quad (5)$$

There is some collector voltage at which $M_n = 1/\gamma\beta$ and $h_{FB} = 1$. As this voltage is approached h_{FE} approaches infinity, and the collector current becomes unbounded.

The voltage at which this occurs, $V_{(BR)CEO}$, is some fraction of the breakdown voltage of the collector junction, and normally a common emitter transistor is operated below this voltage. The region of operation including collector to emitter voltages less than $V_{(BR)CEO}$ will be called the normal region of operation. The avalanche region will comprise greater collector voltages, and operation in this region will be called avalanche mode operation.

At collector voltages above $V_{(BR)CEO}$, h_{FB} is greater than one and h_{FE} is negative. Operation in this region then requires a reverse base current (tending to reverse bias the emitter), and assuming $I_B \gg I_{CBO}$ the collector current is related to the base current by

$$I_C = \frac{-\gamma\beta}{\gamma\beta - 1/M_n} I_B \quad (6)$$

The result is collector characteristics similar to those shown in Figure 1. The incremental collector resistance is negative in the avalanche region.

Stable Operating Points

With a fixed reverse base bias and a collector load resistor R_L two stable states of operation can be obtained. One occurs when the emitter is reverse biased and the only collector current is a reverse leakage current. The other stable state is represented by the intersection of the $I_B = -I$ curve and the load line in Figure 1. The collector voltage in the latter state is somewhat above $V_{(BR)CEO}$. This collector voltage, $V_{CE(on)}$, is that collector voltage at which $M_n = (1/\gamma\beta)/(1 + I_B/I_C)$. The collector voltage while the transistor is off, $V_{CE(off)}$, is equal to V_{CC} if the collector leakage current is neglected. Near the voltage at which the collector junction breaks down this leakage current will rise rapidly with collector voltage, and there is some voltage at which it overcomes the reverse base current and forward biases the emitter. This collector voltage, $V_{(BR)CEX}$, is an upper limit of $V_{CE(off)}$ and is normally close to the breakdown voltage of the

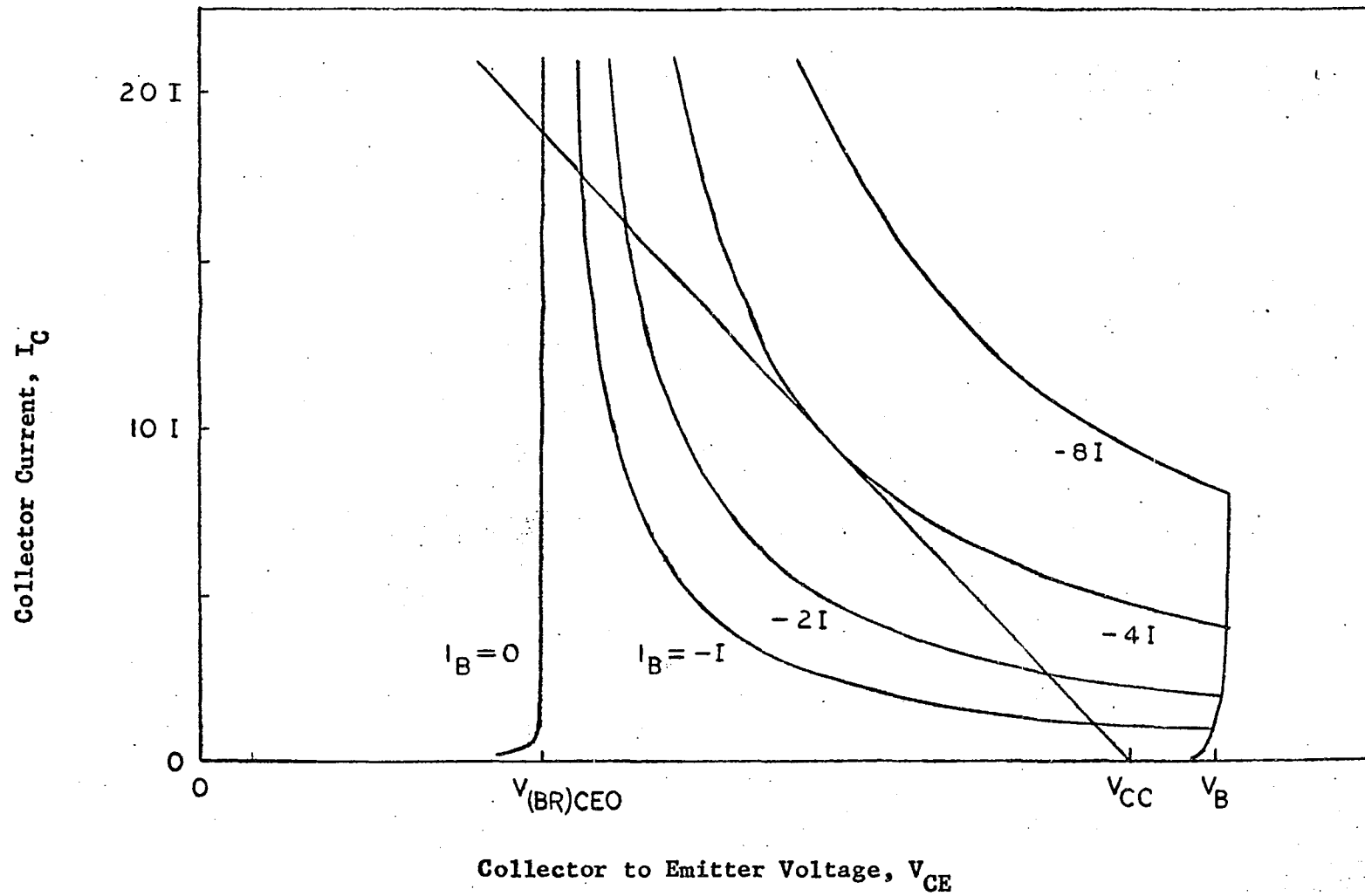


Figure 1. Characteristics of a Transistor in the Avalanche Region

collector junction.

Control

If the transistor is in the non-conducting state in which the emitter is reverse biased it can be switched to the conducting state by removing the reverse bias momentarily. Once the emitter is forward biased internal feedback from collector multiplication completes the turn-on process, and it is not necessary to drive the transistor into the conducting state. This same collector multiplication is also sufficient to overcome a small reverse base current and keep the transistor on even when the reverse bias is reapplied. An avalanche transistor can be triggered into the conducting state by a pulse into either the base or collector. Base triggering is usually the simplest and requires the least trigger power, but collector triggering reduces delay time and jitter problems if these are critical (5).

The problem of returning a transistor to the non-conducting state has generally not been analyzed. Most avalanche transistor circuits accomplish this by removing most of the collector drive after a time and thus permitting the normal base bias current to overcome the avalanche multiplication and turn the transistor off. Figure 1 suggests another method of accomplishing turn-off. Note that if the magnitude of the reverse base current is increased beyond $4I$ the only stable operating point is the non-conducting state. It would then seem that turn-off could be accomplished by a pulse into the base of the transistor. Such a method of turn-off has been used (6) although no real study of such a

method is available.

Basic Theory of Avalanche Multiplication

Any attempt to determine what collector junction will result in an optimum ratio of $V_{CE(off)}$ to $V_{CE(on)}$ requires that there be some method of finding the multiplication factors for any junction if the materials and construction are known. Such a method has evolved over the years, and appears adequate for the purposes of this study. The function of this section is to summarize information which is scattered throughout the literature and not to add to the body of knowledge about secondary ionization.

Miller's Result

One of the more useful approaches utilizes the concept of an ionization rate, α . This ionization rate is considered to be a function of the electric field only and is the number of ionizing collisions per unit distance of travel per carrier. There is no reason to believe that electrons and holes should have the same ionization rates, and in the cases of both silicon and germanium they do not. To distinguish between the two α_n will be used to represent the ionization rate for electrons and α_p the ionization rate for holes.

Miller (3) used this approach and the model of Figure 2. This model represents a junction of width w with a flow of electrons impinging upon it from the left. The following assumptions are necessary.

- (1) The ionization rates of both holes and electrons are functions only of the electric field.

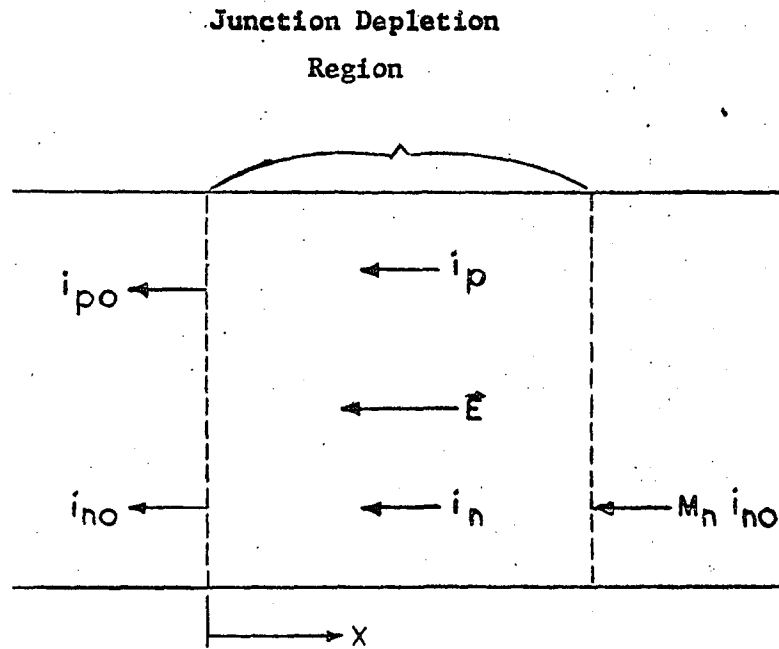


Figure 2. Avalanche Multiplication in a Reverse Biased Junction

- (2) There are no space charge effects from the carriers passing through the junction.
- (3) Recombination within the junction is negligible. Generation by any means other than secondary ionization is negligible.

The width of the junction is dependent upon the material, applied voltage, and doping profile of the junction. The electric field is a function of the construction, applied voltage, and the distance, x , across the junction. Assuming the construction of the junction is known and the applied voltage is held constant the only variable which need be considered is x . The ionization rates are a function of the electric field and thus can be expressed as a function of the distance, x , from the left side of the junction.

The change in the electron current with x is related to the hole and electron currents in the junction by

$$\frac{di_n}{dx} = \alpha_n i_n + \alpha_p i_p . \quad (7)$$

Since the total current is constant everywhere

$$i_n + i_p = M_n i_{no} . \quad (8)$$

These equations can be reduced to a single differential equation in i_p so that

$$\frac{di_p}{dx} - (\alpha_n - \alpha_p) i_p = -\alpha_n M_n i_{no} . \quad (9)$$

The applicable boundary conditions are

$$i_p(0) = (M_n - 1)i_{no} \quad (10)$$

and

$$i_p(w) = 0. \quad (11)$$

From the solution of Equation 9 with these boundary conditions one finds that

$$1 - 1/M_n = \int_0^w \alpha_n \exp\left[-\int_0^x (\alpha_n - \alpha_p) dx'\right] dx. \quad (12)$$

This is the result Miller obtained. M_p is obviously given by the same expression with the roles of α_n and α_p reversed. The $1 - 1/M$ form is often convenient since it compresses all values of M from one to infinity into a range of 0 to 1.

Ionization Rates

By measuring the multiplication rates of various junctions, Equation 12 and the corresponding expression for M_p can be used in finding ionization rates as a function of the electric field. This has been done and the results published (3) (7) (8) (9). The ionization rates for silicon and germanium are shown in Figure 3.

It has been noted by Chynoweth (7) that the ionization rates can be represented empirically by the equation

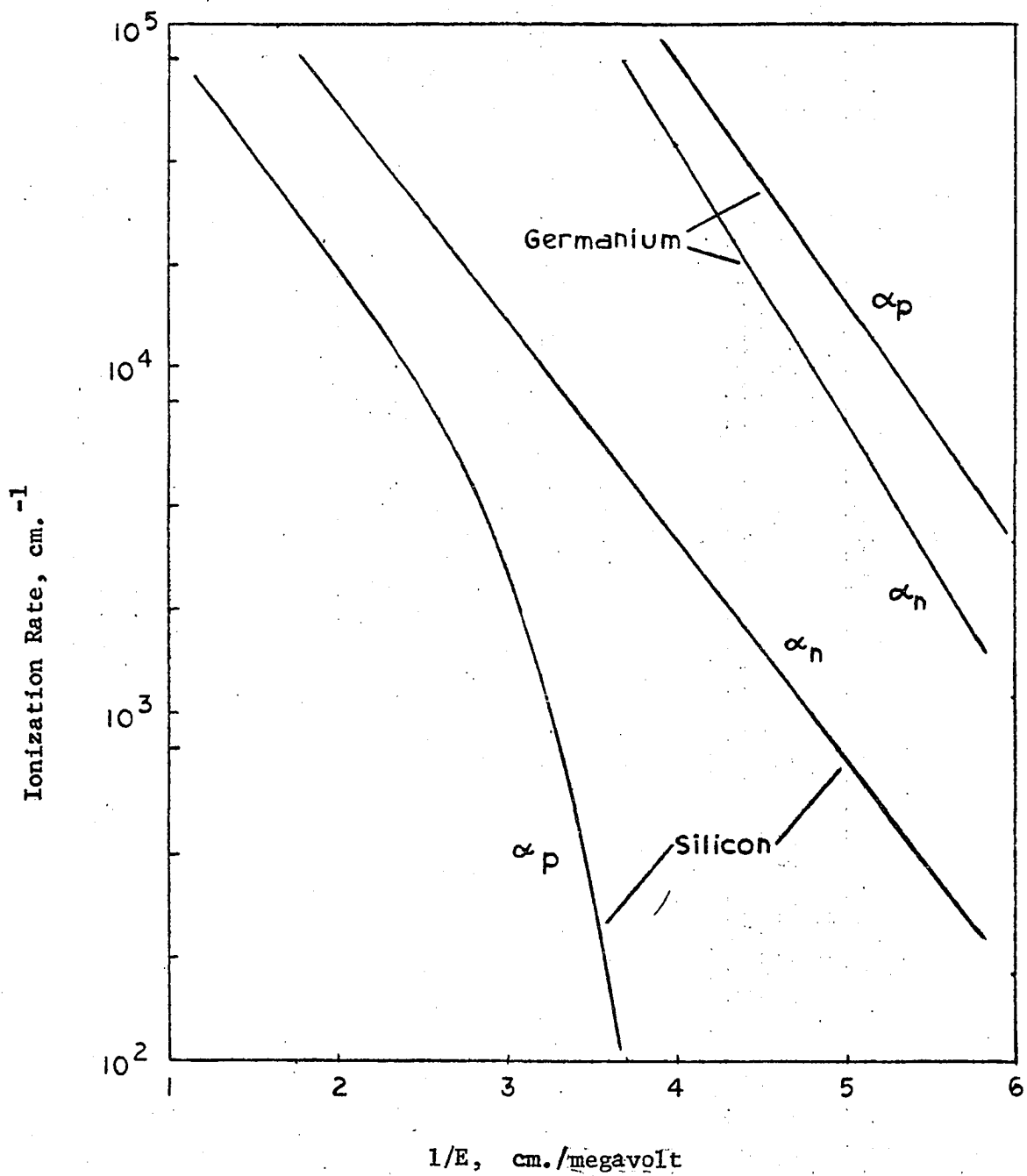


Figure 3. Ionization Rates. [From Chynoweth (7), Moll and Van Overstraeten (8), and Miller (3).]

$$\alpha = a \exp(-b/E). \quad (13)$$

Such an expression corresponds to a straight line in Figure 3. The plot of ionization rate for holes in silicon is the only curve which deviates significantly from this form.

Threshold Effect

There is one more important reservation which must be made concerning the use of this Equation 12. The development of this equation assumed that the ionization rates were a function only of the electric field. Since the ionization is a quantum mechanical process it is not surprising that this assumption will fail for small applied voltages. It has been found that there is some minimum energy which a carrier must have if it is to produce an ionizing collision (10). Unless the total junction potential is sufficient to impart this much energy to the carriers essentially no multiplication will occur. There is then a threshold potential, and, if the total potential is near this threshold, considerably less multiplication will take place than would be predicted by Equation 12 and ionization rates obtained from junctions with a greater applied potential.

In the case of electrons in silicon this threshold appears to be about 1.8 electron volts (8), and a correction must be made for applied voltages of less than 4 volts. Moll (9) has noted that this threshold effect can be accounted for empirically by defining a function

$$f(V - V_T) = \frac{(1 - 1/M)_{\text{measured}}}{(1 - 1/M)_{\text{calculated}}} \quad (14)$$

This function varies as $(V - V_T)^2$, where V is the sum of the applied and built-in potential and V_T is the threshold voltage. Then for M_n of a silicon junction with a built-in voltage of 0.8 volts this function becomes

$$f(V - V_T) = 0.111 (V - 1.8v.), \quad (15)$$

and the correction must be used when V is less than 4.8 volts.

OPTIMUM COLLECTOR MULTIPLICATION

General Considerations

If an avalanche transistor is to be used as a bistable switch the collector voltage during conduction should be made as low as possible when compared to the collector voltage during the time the transistor is turned off. $V_{CE(off)}$ is limited by the breakdown voltage of the collector junction. $V_{CE(on)}$ is that collector voltage at which $M_n = (1/\gamma\beta)/(1 + I_B/I_C)$. In order for this to occur at as low a value of M_n as possible the $\gamma\beta$ product should be as large as possible. This product cannot have a value greater than 1, and it is at least 0.95 in any practical transistor, so very little can be done to further control this quantity. The alternative approach is to design the collector so that the required value of M_n occurs at a lower collector voltage. It is this course which is pursued here.

It is possible to make some observations about multiplication factors at low voltages in light of the curves of Figure 3. For low values of multiplication the exponential term in Equation 12 is essentially 1 and

$$1 - 1/M_n = \int_0^w \alpha_n dx. \quad (16)$$

This is to be expected since there are not enough holes produced at low values of multiplication to cause a significant number of ionizing collisions. The opposite is true near breakdown where M_n is large and there are nearly equal numbers of holes and electrons contributing to

the ionization process. This is why the breakdown voltage predicted by calculation of M_p is the same as that predicted by a calculation of M_n . In fact accurate predictions of breakdown voltages can be made by choosing an average ionization rate and neglecting the difference between holes and electrons.

Since the breakdown voltage is independent of whether holes or electrons enter the junction, Equation 16 shows that the carriers with the higher ionization rate will produce a higher avalanche multiplication factor at low voltages. This dictates the choice of either an NPN silicon transistor or a PNP germanium transistor for avalanche operation. All available information and experience show that silicon junctions have higher multiplication rates at voltages below breakdown than do germanium junctions. The $V_{(BR)CEO}$ ratings published for various types of transistors support this choice since invariably the rating for an NPN silicon transistor is lower compared to the collector breakdown rating than that of any other type of transistor with a comparable breakdown voltage rating. On this basis specific consideration will be given only to M_n in silicon.

The question still remains as to what type of collector junction possible on an NPN silicon transistor will achieve the maximum $V_{CE(off)}/V_{CE(on)}$ ratio. Specifically the effect which the doping profile and the breakdown voltage have upon this ratio must be determined.

First it seems reasonable to restrict the study to junctions which vary monotonically from P-type to N-type silicon. Anything else would present impossible construction difficulties. The usual method of con-

structuring silicon transistors is by double diffusion of N-type silicon. Capacitance measurements on diffused junctions have shown that they behave as graded junctions at low voltages and as step junctions at higher voltages (11). Calculations of the avalanche multiplication factor are considerably simplified if they need be carried out only for linearly graded and step junctions. Since a diffused junction is intermediate to these two types of junctions a good indication of the range of results possible can be obtained by calculating the multiplication for both step and linearly graded junctions.

Calculation of Avalanche Multiplication

Equation 12 is difficult to use as shown. A more useful form has been developed by Moll and Overstraeten (11) by letting $\alpha_p = \gamma\alpha_n$.

Then

$$1 - 1/M_n = \int_0^w \alpha_n \exp\left[\int_0^x (\gamma - 1)\alpha_n dx'\right] dx \quad (17)$$

Treating γ as a constant and noting that the integrand is then a perfect differential this becomes

$$1 - 1/M_n = \frac{1}{1 - \gamma} \left[1 - \exp\left[-(1 - \gamma) \int_0^w \alpha_n dx\right] \right]. \quad (18)$$

This will prove to be a fairly usable form with which to predict M_n . For electric fields above 5×10^5 v./cm. in silicon γ is nearly constant, but it drops off rapidly at lower electric fields. This does not greatly affect the accuracy of Equation 18 since the ionization rate in-

creases very rapidly with electric field in this range, and most of the secondary ionization takes place in that part of the junction where the electric field is near maximum. If the value of γ corresponding to the maximum electric field is chosen, Equation 18 becomes a reasonable approximation which gives good results for most collector voltages (8) (9).

Step Junctions

The electric field in a step junction is shown in Figure 4a. An analytical representation of the field strength is

$$E = \begin{cases} E_m x/x_0, & 0 \leq x \leq x_0 \\ E_m (w - x)/(w - x_0), & x_0 < x \leq w. \end{cases} \quad (19)$$

where E_m is the maximum field in the junction, w is the width of the depletion region and x_0 is the distance from the edge of the depletion layer to the metallurgical junction. By letting $\alpha_n = a_n \exp(-b/E)$ and using the analytical expression of Equation 19 it can readily be shown that

$$\int_0^w \alpha_n dx = \int_0^w a_n \exp(-bw/E_m x) dx. \quad (20)$$

This integral and thus the value of multiplication given by Equation 18 is independent of the value of x_0 . This shows that any two step junctions with the same values for w and E_m (and thus the same total junction po-

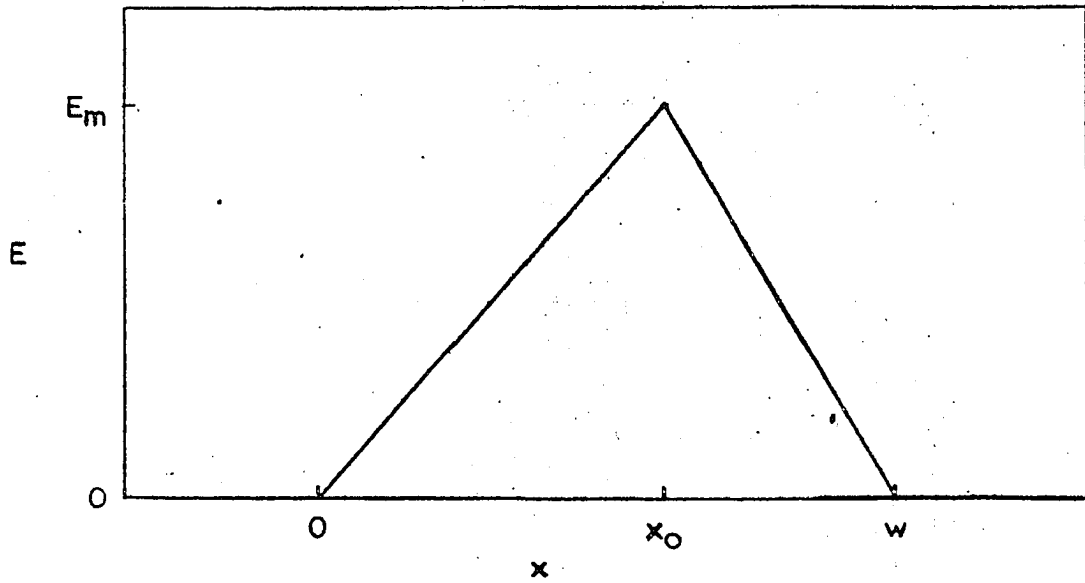


Figure 4 a. Electric Field of a Step Junction

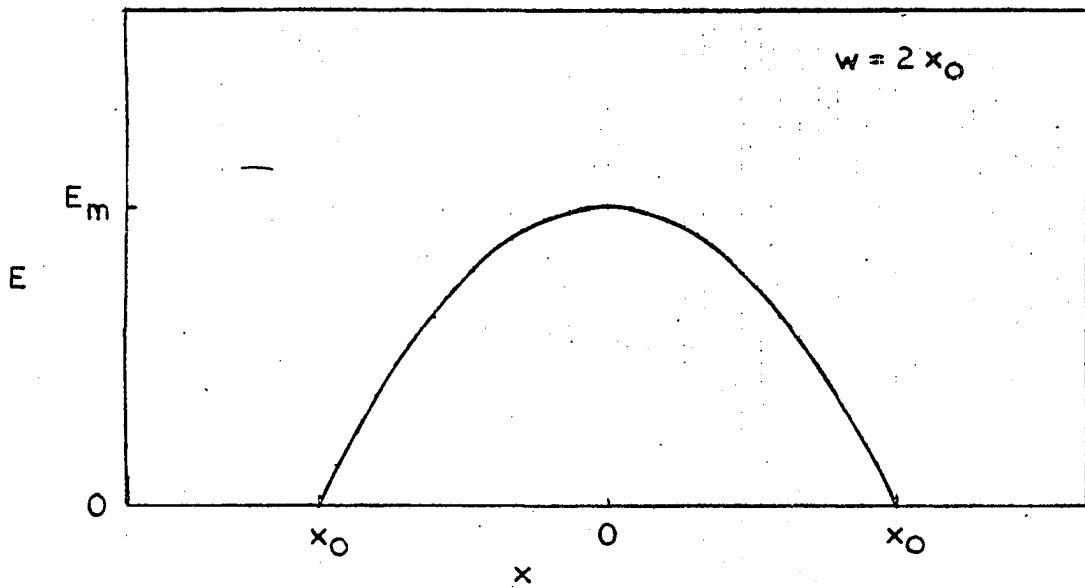


Figure 4 b. Electric Field of a Linearly Graded Junction

tential) will have the same avalanche multiplication factor.

For purposes of multiplication studies a step junction can then be completely characterized by its width constant w_1 . The width constant corresponds to the width of the depletion region when the total junction potential is 1 volt. The depletion region width and maximum field of a step junction as a function of the junction potential are then

$$w = w_1 \sqrt{V} \quad (21)$$

and

$$E_m = 2 \sqrt{V}/w_1. \quad (22)$$

The width constant is related to the construction of the junction by

$$w_1 = \sqrt{2\epsilon/qN} \quad (23)$$

where ϵ is the permittivity of the material, q is the electronic charge, and N is related to the net doping levels of both sides of the junction by $N = 1/N_A + 1/N_D$.

The evaluation of Equation 20 is simplified by writing it as

$$\int_0^w \alpha_n dx = a_n \exp(-b/E_m) \int_0^w \exp\left[(1 - w/x)b/E_m\right] dx. \quad (24)$$

Then by defining

$$w_{\text{eff}}/w = \int_0^1 \exp\left[(1 - 1/z)b/E_m\right] dz \quad (25)$$

an equation of the form

$$\int_0^w \alpha_n dx = \alpha_n(\text{max}) w_{\text{eff}} \quad (26)$$

results. Graphs of w_{eff}/w are available (8) (9), but better accuracy is obtained by evaluating Equation 25 for a few values of b/E_m .

The calculation of M_n for a junction with width constant, w_1 , proceeds as follows. First a value of b/E_m is assumed. Then by noting that $w = \frac{1}{2} w_1^2 E_m$ Equation 26 can be evaluated as

$$\int_0^w \alpha_n dx = a_n \exp(-b/E_m) \frac{w_{\text{eff}}}{w} \left(\frac{1}{2} w_1^2 E_m \right). \quad (27)$$

In silicon the best fit with measured data for electrons is $a_n = 1.6 \pm 0.2 \times 10^6 \text{ cm.}^{-1}$ and $b = 1.65 \times 10^6 \text{ volts/cm.}$ This holds for electric fields from $2 \times 10^5 \text{ volts/cm.}$ to $6.7 \times 10^5 \text{ volts/cm.}$ Next a value of γ corresponding to E_m is used to find $1 - 1/M_n$ from Equation 18. A plot of $\log(1 - 1/M_n)$ vs. $1/E_m$ happens to be nearly a straight line, and only a few choices of b/E_m are needed for each junction. The breakdown voltage and multiplication at any voltage can then be determined from this plot.

Linearly Graded Junctions

The field pattern in a linearly graded junction can be represented analytically as

$$E = E_m \left[1 - (x/x_0)^2 \right]. \quad (28)$$

The procedure for calculating M_n closely parallels that used for step junctions, and is similar to one outlined by Moll (9). Again the junction can be characterized by a width constant. In this case the junction width and maximum field are related to the junction potential by

$$w = w_1 V^{1/3} \quad (29)$$

and

$$E_m = 1.5 V^{2/3} / w_1. \quad (30)$$

The width constant for a graded junction is

$$w_1 = (12 \epsilon / qa)^{1/3} \quad (31)$$

where "a" is the impurity gradient for the junction.

In this case Equation 20 can be written as

$$\int_0^w \alpha_n dx = 2 a_n \exp(-b/E_m) \int_0^{w/2} \exp - \left[\frac{(2x/w)^2}{1 - (2x/w)^2} \right] b/E_m dx. \quad (32)$$

w_{eff} for a graded junction is defined by

$$w_{\text{eff}} / w = \int_0^1 \exp - \frac{z^2}{1 - z^2} b/E_m dz, \quad (33)$$

and the form of Equation 26 can also be used here. Again a value of b/E_m is assumed. In this case $w = w_1 \sqrt{2 w_1 E_m / 3}$, and

$$\int_0^w \alpha_n dx = a_n \exp(-b/E_m) (w_{\text{eff}}/w) (w_1 \sqrt{2 w_1 E_m / 3}) \quad (34)$$

The value of γ corresponding to E_m is used to evaluate Equation 16, and a plot of $\log(1 - 1/M_n)$ versus $1/E_m$ is obtained as before.

Results

Such calculations can be used to find the $V_{(\text{BR})\text{CEX}}/V_{\text{CE}(\text{on})}$ ratio for transistors with various collector junctions. Unfortunately this calculation is complicated by the fact that these voltages depend in part upon the circuit used and parameters of the transistor other than avalanche multiplication. Since only the effect of the collector junction is desired, the breakdown voltage, V_B , of the collector junction and the collector junction voltage, V_M , at which M_n is equal to 1.1 are calculated instead. The first voltage is very close to $V_{(\text{BR})\text{CEX}}$ in most circuits, and, for a transistor with h_{FE} equal to 20 at low voltages and a reverse base current which is 1/20 of the collector current, $V_{\text{CE}(\text{on})}$ is the collector voltage at which M_n is 1.1. The value of V_B/V_M provides a realistic indication of the effect of the collector junction construction on $V_{(\text{BR})\text{CEX}}/V_{\text{CE}(\text{on})}$.

The values of V_M and V_B calculated for step junctions with various values for w_1 are shown in Table 1. Table 2 consists of the same calculations for linearly graded junctions. Figure 5 is a graphical representation of the variation of V_B/V_M with the junction breakdown voltage

Table 1. Calculated V_B and V_M for step junctions

Width Constant w_1 $\mu/\text{volt}^{1/2}$	Breakdown Voltage V_B volts	Voltage at which M_n is 1.1 V_M volts	$\frac{V_B}{V_M}$
0.06	8.2	2.7	3.0
0.08	10.2	3.2	3.2
0.10	12.6	3.7	3.5
0.12	16.0	4.5	3.6
0.15	19.9	5.8	3.4
0.20	27.6	9.6	2.9
0.30	44.8	17.7	2.5

Table 2. Calculated V_B and V_M for Linearly Graded Junctions

Width Constant w_1 $\mu/\text{volt}^{1/3}$	Breakdown Voltage V_B volts	Voltage at which M_n is 1.1 V_M volts	$\frac{V_B}{V_M}$
0.06	6.4	2.6	2.5
0.10	9.3	3.4	2.7
0.15	13.7	5.1	2.7
0.20	17.8	7.2	2.5
0.30	27.3	12.3	2.2
0.40	37.5	17.2	2.2

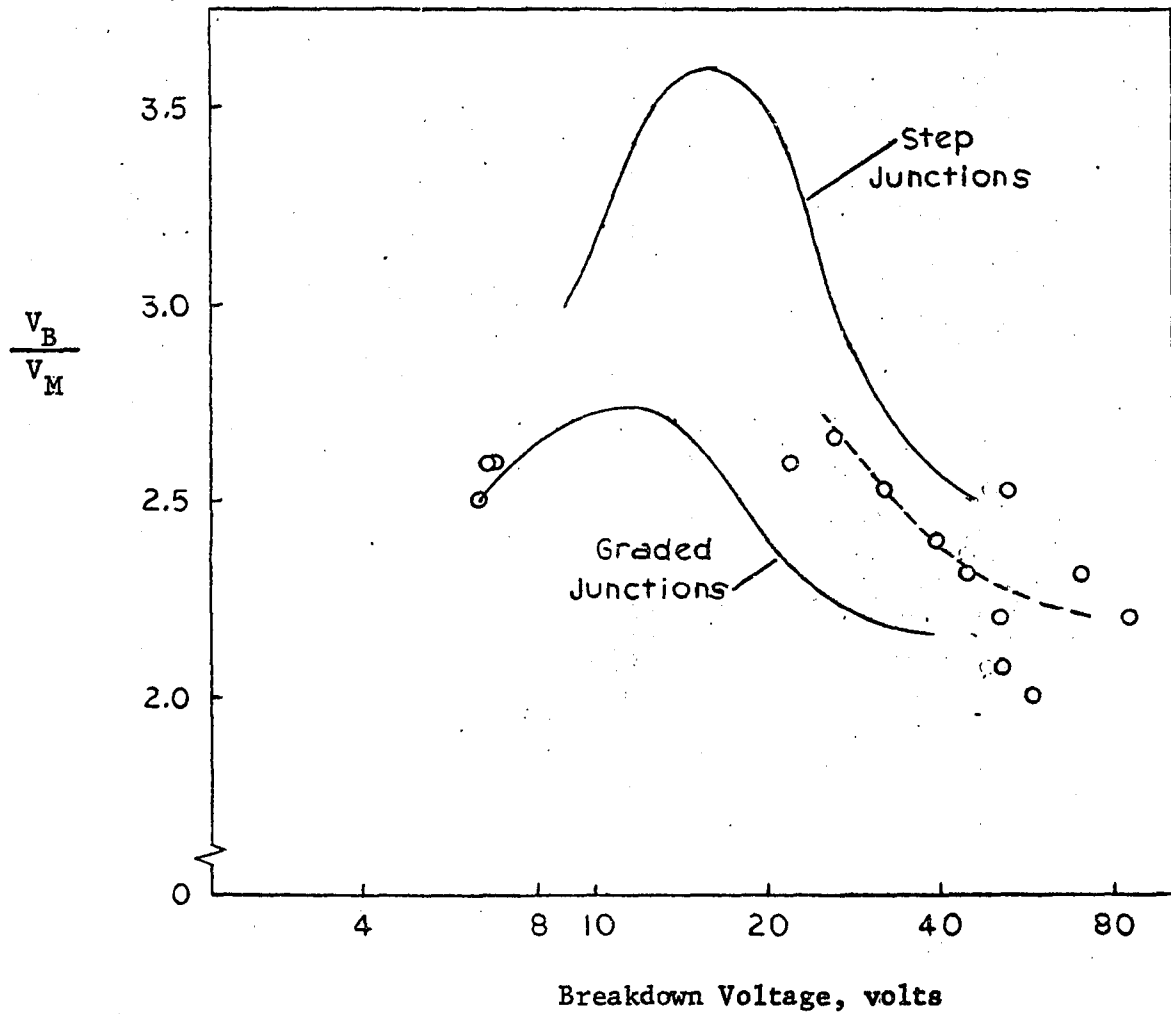


Figure 5. Effect of Breakdown Voltage upon Avalanche Multiplication of Step and Graded Junctions in Silicon. The solid lines are calculated values. The circles and dotted line represent measurements made on diffused junctions.

for both types of junctions.

There are two conclusions which can be drawn at this time. First as shown by Figure 5 a step junction is superior to a graded junction for the collector of an avalanche transistor. Second a collector breakdown voltage somewhat less than that generally found in transistors will result in a maximum value of $V_{(BR)CEX}/V_{CE(on)}$. The optimum collector junction for an avalanche transistor is a step junction with a breakdown voltage of 15 volts. It is interesting to note that Zener breakdown which is caused by internal field emission does not prove to be a practical limitation in the design of an avalanche transistor. The peak value of V_B/V_M for both step and graded junctions occur when V_M is equal to 4 volts. This is the applied potential at which the threshold effect becomes important. Zener breakdown of silicon junctions occurs only in junctions with breakdown voltages less than 8 volts. Because of the threshold effect any reduction of the avalanche breakdown voltage to less than 8 volts would not appreciably reduce $V_{CE(on)}$. It is this threshold effect rather than Zener breakdown which imposes a lower limit on the voltage range of avalanche transistors.

The formation of a junction by an alloying process results in a very good step junction. The diffusion process used with silicon transistors will never result in a true step junction. The nearest approximation will result if a very heavy diffusion which extends only a short distance into the crystal is made. Then a large part of the depletion region may occur in the part of the crystal which was not reached by the diffusion, and the field pattern may approach that found in a step junction in which one side of the junction is doped very heavily. This type of

diffusion for a collector will be made only in transistors which are intended for very high frequency operation, as this tends to create a very narrow base layer. At the same time relatively low resistivity silicon must be used for collector material so that the junction is formed near the surface of the crystal, and this tends to cause low breakdown voltages.

Measurements of Collector Multiplication

Collector multiplication can be found by measuring h_{FB} at various voltages and assuming that any increase above the value measured at a couple of volts is due to avalanche multiplication. Actually the base transport factor will increase slightly with an increase in collector voltage, but this introduces appreciable error only at low values of multiplication and does not greatly affect a measurement of V_M . Measurement of very high values of multiplication is also impossible as the transistor becomes unstable and begins to oscillate. The use of low current levels helps, but it is seldom possible to measure multiplication factors above 2 or 3.

Measurements were made on several silicon planar transistors. Only junctions which had stable breakdown voltages and did not have excessive noise or other signs of gross crystal defects were used. Emitter junctions were used to obtain measurements on junctions with a low breakdown voltage. Not all emitter junctions can be used since breakdown may occur in regions of small reverse mode current flow. The results of these measurements are shown in Table 3 and are also included

Table 3. Results of Transistor Multiplication Measurements

Transistor Type	Unit	V_B	V_M	V_B / V_M
2N709	2	26 v.	9.8 v.	2.7
2N709	6	32 v.	12.6 v.	2.5
2N709	7	39 v.	17.4 v.	2.4
2N709	9	52 v.	25 v.	2.1
2N709	10	51 v.	20 v.	2.5
2N709	11	44 v.	19 v.	2.3
2N709	12	23 v.	8.9 v.	2.6
2N709	13	65 v.	28 v.	2.3
2N708	1	55 v.	28 v.	2.0
2N708	2	76 v.	34 v.	2.2
2N708	3	57 v.	26 v.	2.3
SL ^a	1	6.5 v.	2.5 v.	2.6
SL ^a	2	6.7 v.	2.5 v.	2.7
SL ^a	3	6.5 v.	2.5 v.	2.6

^aMeasurements on emitters of unnumbered samples of saturating logic silicon transistors.

in Figure 5 for comparison with the calculated curves.

These measurements are consistent with and support the calculations. It was anticipated that they should fall into an intermediate range between the values calculated for step junctions and graded junctions, and they do. The general trend is for the V_B/V_S ratio to increase as the collector breakdown voltage becomes less, and, although none were found to have as low a breakdown voltage as desired, it would appear that transistors with a V_B to V_S ratio of 3 or better could easily be made. Especially at higher voltages there is considerable variation among transistors of nearly the same breakdown voltage. Variations in the normal manufacturing procedures are enough that two junctions with identical breakdown voltages can be far from identical. Another consideration is the presence of microplasmas at voltages below breakdown which will cause some variation in multiplication. Although most junctions have small imperfections which lead to the formation of microplasmas (12) these seldom have any major effect on the multiplication factor except at low current levels (13). Gross defects can lead to larger microplasmas which can be identified by the noise they produce (14). In 2 units there were defects large enough to cause secondary breakdown at only a few ma. of collector current. Such transistors are, of course, completely unsatisfactory for use in avalanche mode operation.

Analytical Approximations for M

Early in the study of avalanche multiplication the empirical formula

$$M = 1 / \left[1 - (V/V_B)^n \right] \quad (35)$$

was proposed (3). This has been very widely used and has been utilized in the analysis of avalanche transistors. This formula is, at best, only an approximation and has no theoretical justification. A comparison between this formula and the values predicted and measured for M_n in silicon junctions is of considerable interest in any analysis of avalanche transistor circuits utilizing NPN silicon transistors.

Since the $1 - 1/M$ form is more convenient for such work, first note that the above empirical formula can be written as

$$1 - 1/M = (V/V_B)^n \quad (36)$$

Figure 6 shows plots of $1 - 1/M_n$ as calculated for the 27.6 volt step junction and the 27.3 volt graded junction, and as measured for the collector junction of unit 2 of the 2N709's which has a breakdown voltage of 26 volts. No choice of n in Equation 36 will provide good agreement with the empirical form over the range of interest for avalanche transistors. In fact the plots are nearly linear throughout the region of high multiplication. Similar plots of calculated and measured multiplication for other junctions show the same pattern.

A better match over the range of interest is a straight line function of the form

$$1 - 1/M_n = \frac{V - V_o}{V_B - V_o} \quad (37)$$

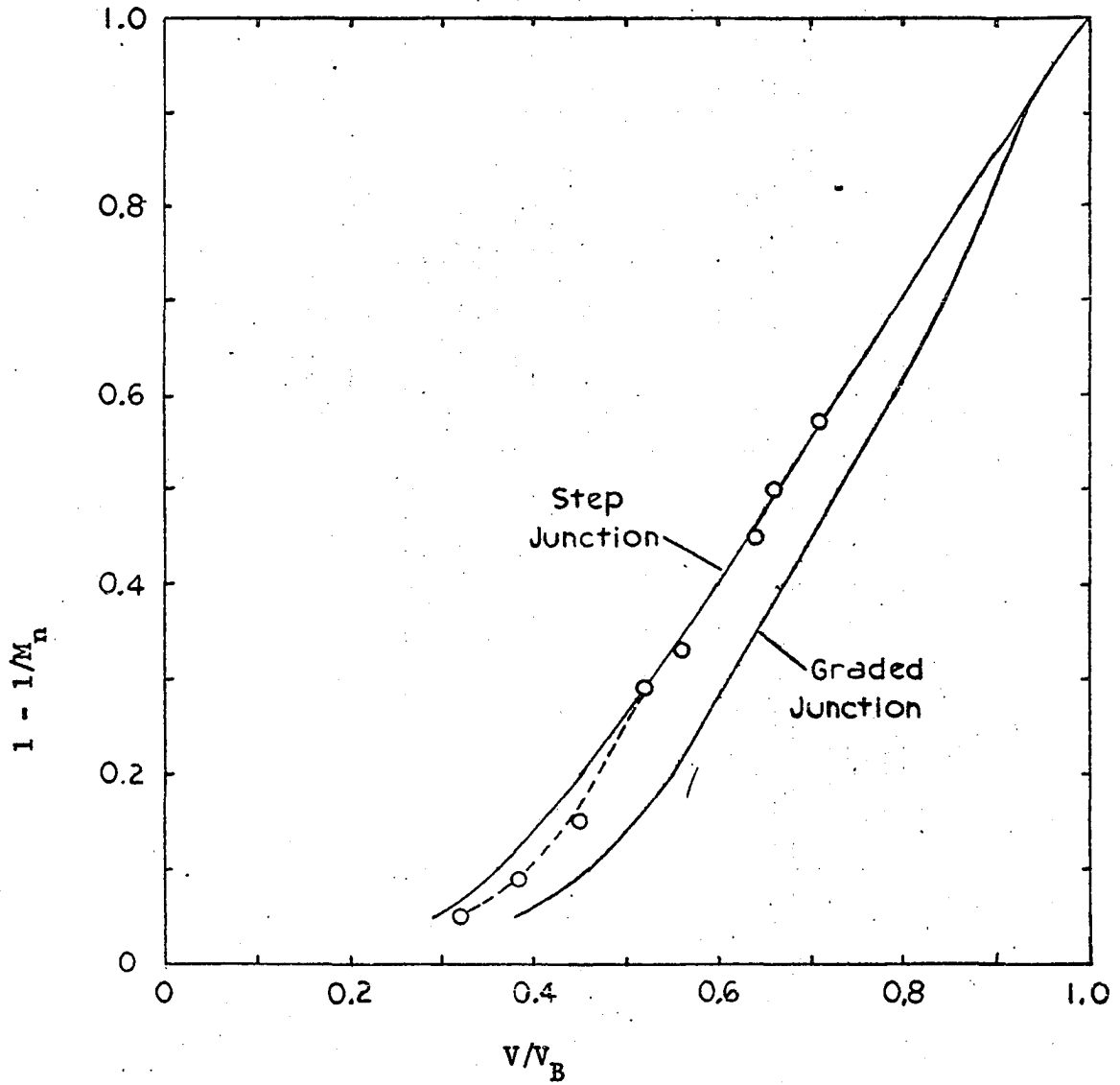


Figure 6. Electron Multiplication in Silicon Junctions. The solid lines represent calculated data. The circles and dotted line are from measurements made upon a diffused junction.

where V_0 is chosen to provide the best match with multiplication data. In the case of the 26 volt collector junction considered in detail here a choice of 8.8 volts for V_0 provides a very good fit for collector voltages above 10 volts. At lower voltages it is, of course, unusable, and it is very possible that in this range an expression of the form of Equation 36 will be more satisfactory. An alternate form of Equation 37 is

$$M_n = \frac{V_B - V_0}{V_B - V}, \quad (38)$$

and this may be more useful in some cases.

It is of interest to note that the curve of measured multiplication in Figure 6 is nearly identical to the calculated curve for voltages above 13 volts indicating that in this range the junction acts as a step junction.

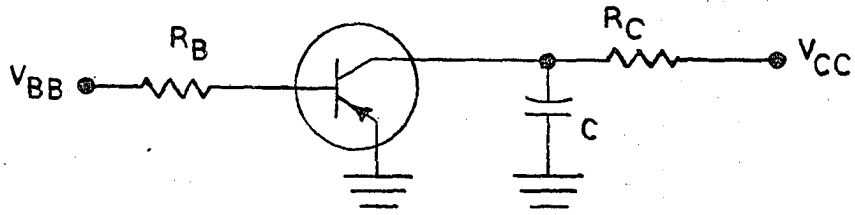
TURN-ON OF AVALANCHE TRANSISTORS

Previous Work

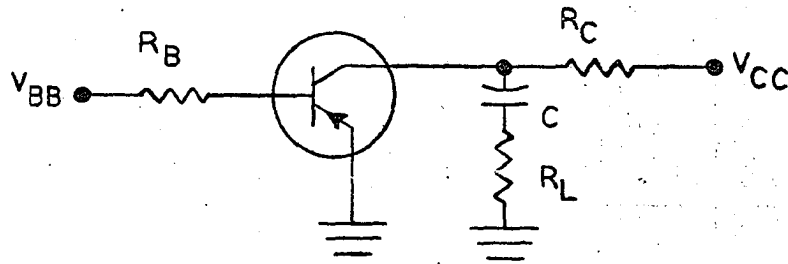
All previous studies of avalanche transistor operation have dealt with alloy junction germanium transistors. It is logical that some differences will be observed in the operation of silicon diffused transistors. The question to be answered is just how they will differ and what modifications in previous methods of analysis are needed to allow for these differences.

Three basic avalanche transistor switching circuits are shown in Figure 7. The first of these is a relaxation oscillator which drives a capacitive load during turn-on. In such a circuit a value of V_{CC} greater than the collector breakdown voltage is used. Capacitor C first charges through R_C to the collector breakdown voltage. The resulting collector current overcomes the reverse bias applied through R_B , forward biases the emitter junction and turns the transistor on. A study of this circuit by Hamilton, Gibbons, and Schockley (15) using charge analysis demonstrated some interesting properties.

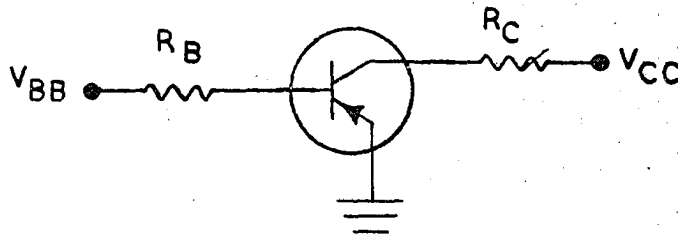
During turn-on and while the transistor is operating in the avalanche mode the collector current increases rapidly. This is accompanied by a build-up of minority carrier charge in the base. After the collector voltage has dropped to a level at which collector multiplication is no longer significant this charge remains forcing the transistor to continue to conduct and, thus, continue to discharge the capacitor C. If C is large enough compared to the collector to base



a. Avalanche Relaxation Oscillator



b. Modified to Create a Pulse Generator



c. Operation with a Resistive Load

Figure 7. Basic Avalanche Transistor Circuits

capacitance of the transistor, sufficient charge will have been built up to completely discharge the capacitor and drive the transistor into saturation. The reverse bias on the base then reverse biases the emitter, turning the transistor off. The collector supply recharges C and the process is repeated. Assuming that R_C and R_B are large enough that the currents through them can be neglected during switching, a fairly simple model is possible assuming uniform currents and geometry for the transistor.

A slight modification of this circuit as shown in Figure 7b permits its use as a pulse generator. The operation is basically the same if the load resistance is kept small and a voltage proportional to the collector current appears across this resistor. Such a circuit can be used to produce very short pulses with very fast rise times. The output voltage is naturally much less than the change in collector voltage, and most of the energy stored in the capacitor is dissipated in the transistor. Also duty cycle is limited by the necessity of recharging the capacitor, C, before another pulse can be produced.

By discharging a coaxial delay line rather than a capacitor into the load some of these difficulties can be overcome. Pulse shape is very much improved and the pulse length is easily controlled by controlling line length. During turn-on such a circuit is essentially switching a resistive load as shown in Figure 7c. An analysis of a delay line pulse generator by Hamilton (16) provides a method of analyzing circuits where a resistive load occurs. This shows that the rise time of the collector current is about 4 times that obtained for

the same transistor with a capacitive load.

Methods of Analysis

The analysis in the case of each of these circuits has utilized a diffusion model for the transistor. In equilibrium the collector current is related to the stored minority carrier charge, q_s , in the base by

$$I_C = q_s / \tau_b \quad (39)$$

where τ_b is the average transit time for a carrier from emitter to collector. Use of this formula for non-equilibrium conditions corresponds to the use of a single pole representation for h_{fe} in small signal models of transistor. For an alloy junction transistor τ_b is very dependent upon the collector voltage. Much of the higher speed operation of such transistors in the avalanche mode is due to the much smaller value which τ_b has at voltages near the punch through voltage of the transistor. There are, in fact, advantages to the use of a transistor in which the punch through voltage is less than the avalanche breakdown voltage of the collector (5).

The models used for these transistors assumed uniform current distributions across the junction area of the transistor and neglected the possibility of lateral fields in the base during switching. It will be impossible to neglect this effect on the transistors used in this study. Also avalanche multiplication for such transistors has been approximated by the empirical formula of Equation 35. Although this

proved acceptable for the transistors studied it seems unlikely that this will carry over to the NPN silicon transistors of major interest at this time.

Experiment

Transistors Used

The reasons for the choice of 2N709's for the experimental portions of this study have already been discussed. At this time a more detailed consideration of their construction and characteristics is in order. The 2N709 is an NPN silicon planar epitaxial transistor designed for low level saturated switching applications. It utilizes a simple geometry as shown in Figure 8, and junction areas are kept as small as possible so as to minimize junction capacitance. The details of construction were supplied by Fairchild Semiconductor Corporation and will be referred to as needed.

There are several significant aspects to the geometry as shown in Figure 8. The area of the emitter junction is only a small fraction of that of the collector junction. Most of the capacitance of the collector junction is to the bulk base region rather than to the active base region which is covered by the emitter. During the time the transistor is turning on, for example, the current resulting from this capacitance must flow laterally in the base material if it is to reach the emitter junction. Also there is a significant collector capacitance not associated with the collector junction. The case is connected electrically to the collector, and any capacitance from, say, the base

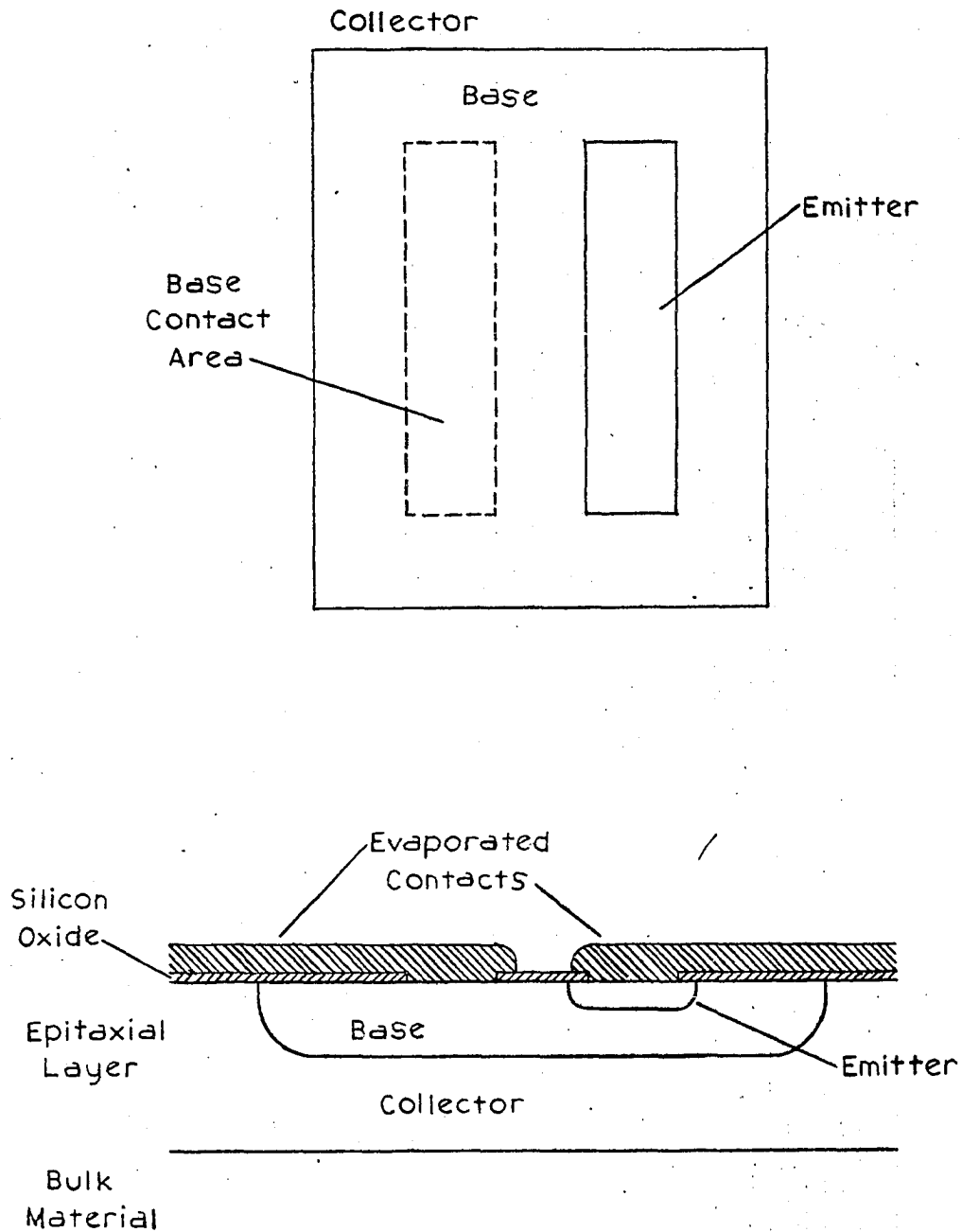


Figure 8. Construction of 2N709 Transistor

lead to the case is also to the collector. In addition the evaporated contacts for the base and emitter extend over the collector portion of the crystal, and this results in a capacitive coupling. Capacitance measurements on the transistors show that the collector capacitance not related to the collector junction is about 1.6 pf. and is equally distributed between the emitter and base leads. This additional 0.8 pf. capacitance from collector to base results in current during turn-on which is coupled to the base contact and must travel laterally through the base to reach the emitter.

Since lateral base currents are certain to occur, a measurement of the resistance which they will encounter is needed. There are several ways of measuring the base spreading resistance, r_b , of a transistor. Since a common use of this parameter is to define an element in the high frequency equivalent circuit of a transistor, a measurement of the resistive part of the input impedance at high frequencies is often used. A more applicable method for the present purpose is to measure both the forward current gain and mutual transconductance of the transistor at high current levels. This can easily be done on a curve tracer and the base spreading resistance can be determined from these measurements. If there were no base resistance the mutual transconductance would be

$$g_m = I_C q / 2kT \quad (40)$$

where k is Boltzman's constant, q the electronic charge and T the temperature in degrees Kelvin. Allowing for the base spreading resistance,

$$g_m = 1/(r_b/h_{fe} + kT/qI_C), \quad (41)$$

and thus

$$r_b = h_{fe} (1/g_m - kT/qI_C). \quad (42)$$

There are two components to the base spreading resistance in these transistors. The first is the resistance, r_{b1} , from the edge of the active base region to the base contact. The second is an average resistance r_{b2} , from points within the active base region to the bulk base region. An idea of the magnitude of each would be useful. The emitter junction of all units exhibited breakdown at about 5 volts. This is most likely a Zener breakdown and occurs at the edges of the emitter junction since this is the point of contact with the most heavily doped part of the base. A good measure of r_{b1} can then be obtained by biasing the emitter junction in breakdown and measuring the series resistance. r_{b2} can then be found as the difference between r_b and r_{b1} .

Table 4. Base Resistance Measurements

Unit	r_b	r_{b1}	r_{b2}
2	59 ohms	32 ohms	27 ohms
6	100 ohms	33 ohms	67 ohms
7	100 ohms	42 ohms	58 ohms
9	105 ohms	35 ohms	65 ohms
10	75 ohms	30 ohms	45 ohms
11	75 ohms	39 ohms	36 ohms
12	90 ohms	33 ohms	57 ohms
13	105 ohms	44 ohms	61 ohms

Although multiplication measurements upon the collector junctions of these transistors indicate the field patterns are more in accordance with a step junction at the higher collector voltages, an estimate of the doping profile of the collector junction is needed to support this observation. The information on manufacture shows a donor density of $6 \times 10^{16} \text{ cm.}^{-3}$ for the epitaxial layer. The base diffusion has a gaussian distribution and an acceptor density of 1 to 2×10^{19} at the surface of the bulk base region. The measurements of r_{b1} correspond to a sheet resistivity for the bulk base region of 150 to 200 ohms. If the collector junction is formed 2μ from the surface with a surface doping level of 10^{19} cm.^{-3} , the sheet resistance will be 170 ohms. Then the net impurity level in the vicinity of the collector junction will be given by

$$N_A - N_D = 6 \times 10^{16} \left[1 - \exp(-x/0.2\mu) \right]. \quad (42)$$

Equation 42 can be obtained by choosing a gaussian curve to give the proper acceptor density at the surface and at the collector junction and then rewriting it in terms of the distance, x , from the collector junction into the collector material. It can be seen that the doping level rises rapidly in the direction of the base and rapidly approaches that of the epitaxial layer on the collector side. Since the junction depletion region will be at least 0.4μ in width at voltages in the avalanche region most of the depletion region will occur on the collector side of the junction, and in this voltage range the properties of a step junction would be expected. By way of comparison a step junction with this

collector doping level would have a breakdown voltage of about 20 volts.

Measurements of Turn-on

The switching speeds attained with these transistors in avalanche mode operation are well beyond the capability of any conventional oscilloscope. It was necessary to use a sampling oscilloscope, and even this was not entirely satisfactory. The fast rise pulse generator used is of a mercury relay type and has a rise time of 0.25 nsec. After passing through the delay cable necessary with a sampling system the rise time should be close to 0.3 nsec. The sampling oscilloscope used cannot measure rise times this fast and thus this was measured as a 0.7 nsec. rise time.

At the switching speeds encountered, component placement and end to end capacitance of resistors are important considerations. All passive circuits were checked by observing their response with a known pulse from the pulse generator. In some cases it was necessary to add capacitors to voltage dividers to compensate for the capacitance of the resistors used. Circuit configurations were chosen, in part, because of the need to include the 50 ohm input impedance of the sampling oscilloscope into the circuit.

The circuit used to measure waveforms during turn-on is shown in Figure 9. The 120 pf. capacitor is charged by V_{CC} through the 10 K. resistor. During switching this resistor has a negligible effect and the collector load is a resistance of $R_C + 50$ ohms. The discharging time constant for the 120 pf. capacitor is 32 nsec. with the smallest value used for R_C , thus it serves as a good coupling capacitor during

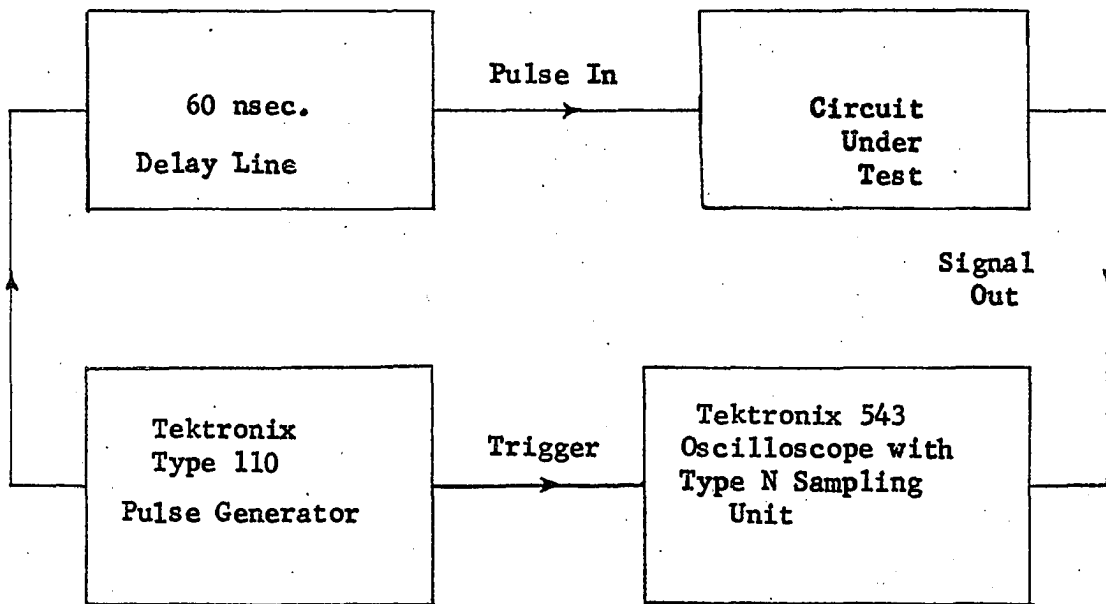
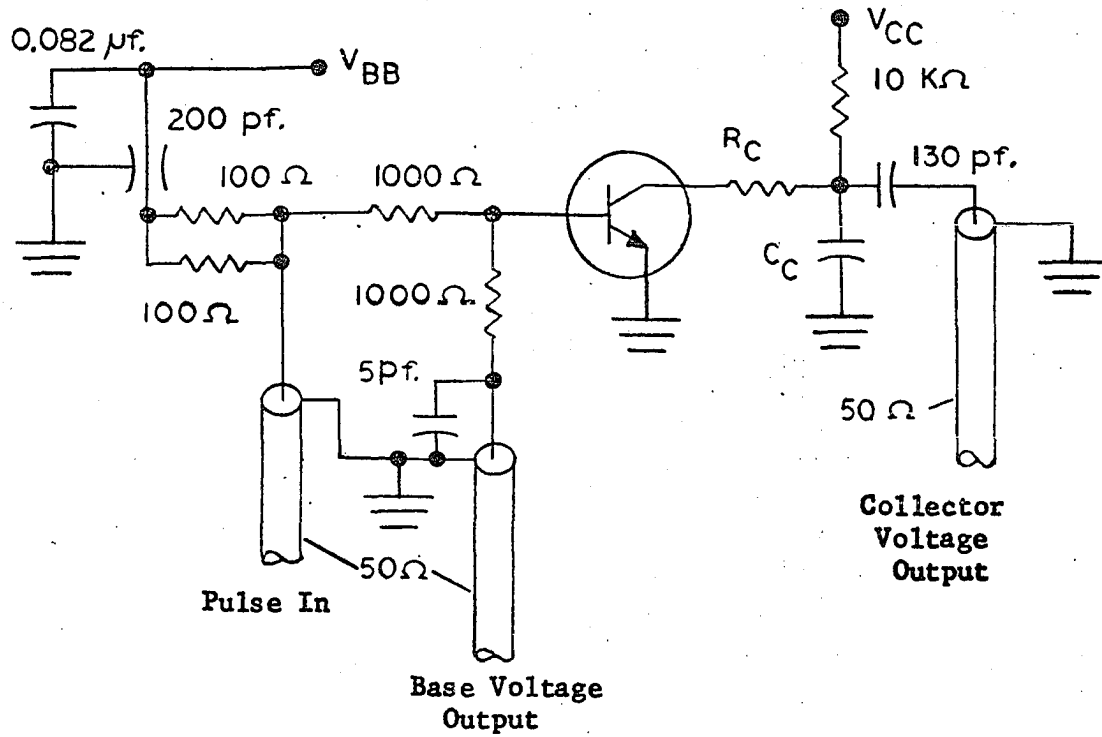


Figure 9. Circuit for Measuring Turn-on of Avalanche Transistors

turn-on. A small capacitor, C_c , was sometimes needed to compensate for the capacitance of the resistor used for R_c .

V_{BB} is made a good a.c. ground by the 200 pf. feed-through capacitor shunted with the 0.082 μ f. tantalic capacitor. This makes it possible to terminate the input pulse line with 50 ohms to this voltage rather than to ground, and it is unnecessary to capacitively couple the input pulse to the circuit. The input pulse is coupled to the base of the transistor through a 1 K. resistor. A second 1 K. resistor from the base to the input of a 50 ohm line is used to measure the base voltage. The 5 pf. capacitor across the input to this line compensates for the capacitance of the 1 K. resistor. This line is terminated with a 50 ohm load during measurement of the collector voltage, and the output line from the collector is likewise terminated during measurement of the base voltage.

Measurements were taken first with a 1 K. resistor for R_c and a 5 pf. capacitor for C_c . The collector load impedance is then that of a 1050 ohm resistor shunted by a 0.2 pf. capacitor. The 1 K. resistor used for R_c was later replaced with a 220 ohm resistor, and the 5 pf. capacitor was removed. Although only a very small duty cycle was used, it was necessary to limit the collector current in the conducting state to around 50 ma. to avoid damage to the transistors.

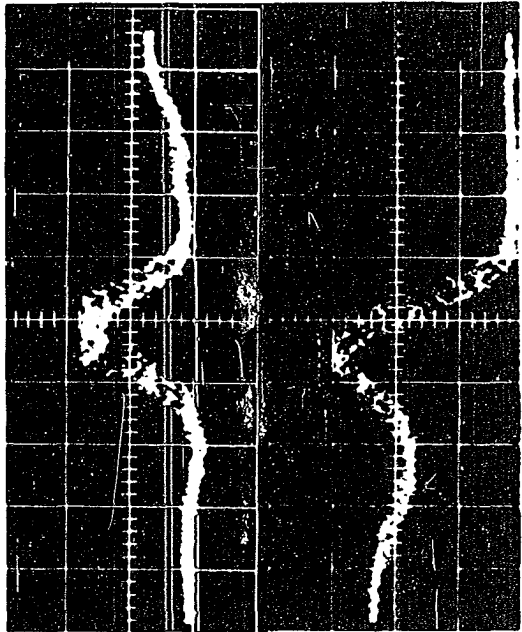
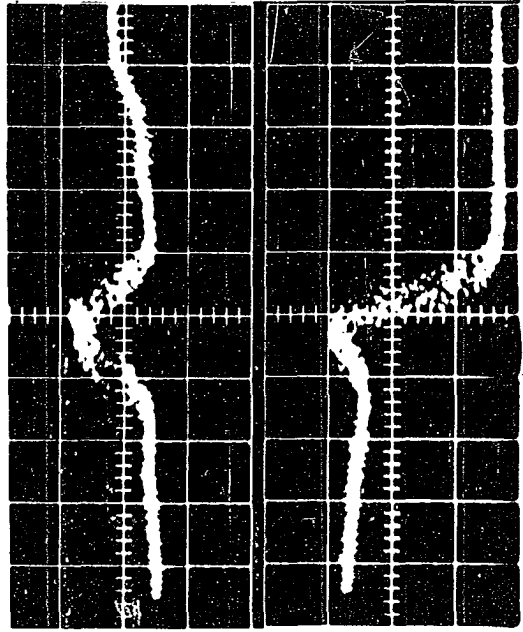
The collector and base voltages during turn-on of unit 12 with both the 1050 ohm load and the 270 ohm load are shown in Figures 10 and 11. The collector voltage is typified by an overshoot and a slight amount of ringing. The application of a pulse generator to the same collector

Figure 10. Avalanche Turn-on with a 1050 ohm Collector Load

The collector waveform is shown in the upper trace and the base waveform in the lower trace. The vertical scale is 6.6 volts/cm. and 2.1 volts/cm. respectively while the horizontal time scale is 1 nsec./cm. The transistor is unit 12 of the 2N709's and has a collector breakdown voltage of 23 volts. The initial values of the voltages shown are 21 volts at the collector and -0.5 volts at the base, and a trigger pulse of 4 volts is used.

Figure 11. Avalanche Turn-on with a 270 Ohm Collector Load

The collector waveform is shown in the upper trace and the base waveform in the lower trace. The vertical scale is 5.4 volts/cm. and 2.1 volts/cm. respectively while the horizontal time scale is 1 nsec./cm. The transistor is unit 12 of the 2N709's and has a collector breakdown voltage of 23 volts. The initial values of the voltages shown are 21 volts at the collector and -0.5 volts at the base, and a trigger pulse of 4 volts is used.



circuits showed no signs of this ringing from the passive circuit alone, thus it must be related to the action of the transistor. Also during turn-on there is a large negative spike in the base voltage which is due to the collector to base capacitance of the transistor.

The limitations of the sampling oscilloscope are apparent in these photographs. The rise times shown are either at the resolution limit of the oscilloscope or very close to it. There is a 0.4 nsec. jitter in the triggering of the sampling pulse which shows up as a broadening of the horizontal lines. This time jitter probably results from the use of an avalanche transistor in the oscilloscope to generate the sampling pulse. The transistor used for this purpose is an alloy junction germanium transistor and it is collector triggered. Although collector triggering should reduce jitter, the lack of additional jitter from the transistor being tested indicates that a silicon transistor which is base triggered will exhibit less jitter than the germanium transistor which is collector triggered.

Analysis

The collector waveform can be explained in this way. The internal capacitance from collector to emitter along with the capacitance of R_C and any wiring capacitance result in a load which is partly capacitive. Altogether there will be more than 1 pf. from collector to ground. This is enough to cause the initial transient to be somewhat like that which occurs when a purely capacitive load is switched. Meanwhile the negative going collector voltage is coupled to the base by the collector

to base capacitance. Since this capacitance is, for the most part, to either the base contact or to the bulk base region rather than to the active base region it is somewhat isolated from the active base region by the base spreading resistance. Only after turn-on is nearly complete is this negative base voltage able to overcome avalanche multiplication.

The base waveform during turn-on shows that the effect of transverse fields in the base cannot be neglected in this type of transistor. Were the entire base region at the potential of the base terminal, the emitter would be reverse biased and the transistor turned off. Since the transistor continues to conduct, at least part of the emitter must be forward biased, but the full area of the emitter is not being used. One measure of the extent of this pinch-in effect is the increase in the base spreading resistance during turn-on. The transistor used to obtain the photograph of Figure 11 has a collector to base capacitance which averages 1.3 pf. over the voltage range through which switching occurs. The rate of change of the collector voltage is, again as an average, 12 volts/nsec. The capacitive current from collector to base is then 16 ma. and opposes the turn-on process. This introduces a negative spike in the base waveform which is 2.1 volts in magnitude. The triggering pulse and base circuit impedance overcome about 5 of the 16 ma., so, if the entire current is assumed to be coupled to the base terminal, the base spreading resistance must be at least 200 ohms. Since r_b in normal operation was measured as 90 ohms it has more than doubled. This increase in the base spreading resistance is evidence

that the area in the transistor through which the current is flowing has been constricted to an area much less than the total emitter area by the capacitive feedback to the base.

A moderate amount of pinch-in with negative base currents has previously been noted (17). This is the basis for some derating of allowed power dissipation when the transistor is used in the avalanche mode. This sharply negative base voltage during turn-on, however, has either gone unnoticed or has been noticed but not reported.

Avalanche Feedback

Avalanche multiplication is the driving force which overcomes the capacitive feedback from collector to base and turns the transistor on. A major reason for the fast switching times possible in avalanche mode operation is the fact that the positive feedback from avalanche multiplication is produced directly within the crystal and is not limited by base resistance effects.

This can be demonstrated by considering the effect of avalanche multiplication upon the collector current density under the following assumptions.

- (1) The electrons injected into the base from the emitter are transported to the collector only by the built-in field in the base region.
- (2) There are no transverse fields or other effects which cause any transverse flow of electrons in the base region.
- (3) Reverse leakage current densities are small and can be neglected.

- (4) The potential across the collector junction remains constant so that there are no effects from the collector transition capacitance or changes in M_n .
- (5) The influence of the base transit time, τ_b , is limited to a storage of minority charge carriers in the base corresponding to a charge per unit area of

$$\sigma_s = \gamma\beta j_E \tau_b . \quad (43)$$

- (6) Charge neutrality is maintained in the base, and the effect of the emitter transition capacitance is negligible.

The second and fourth assumptions in particular will not be met during the time an avalanche transistor is switching, but finding the effect of avalanche multiplication under these conditions will be helpful in determining its effect during switching.

The collector current density at any point is then related to the current density at the corresponding point in the emitter by

$$j_C = \gamma\beta M_n j_E . \quad (44)$$

The collector current entering the base region consists of both a hole and an electron current. The electron current is due to the injection of electrons into the base and this current density is

$$j_{Cn} = \gamma\beta j_E . \quad (45)$$

The hole current density results from avalanche multiplication and is

$$j_{Ch} = \gamma\beta (M_n - 1) j_E . \quad (46)$$

These holes entering the base must either be removed by a transverse base current, recombination, and the hole component of the emitter current, or they must remain in the base region and result in an increase in σ_s . If the transistor is operating in the avalanche region the latter will occur, and the stored base charge is increased by

$$\frac{d\sigma_s}{dt} = j_{Ch} + (1 - \gamma\beta) j_E . \quad (47)$$

The effect of the emitter transition capacitance can be included if σ_s is redefined to include the charge stored in the emitter transition capacitance and τ_b redefined to include the time constant of the emitter junction. This along with the use of Equation 43 for non-constant emitter currents corresponds to the single pole approximation usually made for h_{fe} of a transistor.

By substituting j_{Ch} from Equation 46 into Equation 47 one finds

$$\frac{d\sigma_s}{dt} = (\gamma\beta M_n - 1) j_E . \quad (48)$$

After substituting from Equation 44 this becomes

$$\frac{dj_E}{dt} = \frac{1}{\tau_b} (M_n - 1/\gamma\beta) j_E . \quad (49)$$

Treating M_n as a constant the solution for j_E is

$$j_E = j_{E0} \exp \left[(M_n - 1/\gamma\beta) t/\tau_b \right]. \quad (50)$$

During turn-on the collector voltage will be changing, and M_n will not be constant. For this reason the result of Equation 50 serves only to show that so long as M_n is large compared to 1 there will be a strong positive feedback which will rapidly turn the transistor on. By solving for the stored charge rather than the emitter current density, the result is

$$\sigma_s = \sigma_{s0} \exp \left[(M_n - 1/\gamma\beta) t/\tau_b \right] \quad (51)$$

which is, of course, subject to the same limitation.

Base Resistance Effects

Experimental evidence of a pinch-in effect on the area actually conducting has already been noted. The reason this occurs is that the negative feedback from the collector capacitance has its primary effect at the periphery of the conducting region. Here it is strong enough to overcome the positive feedback of collector avalanche multiplication and reverse bias the emitter junction at this point. During turn-on the emitter at the periphery of the conducting area is continually being reverse biased and the current flow forced into a continually smaller area. While a precise analysis is not practical due to the large number of variables involved, the effect can easily be demonstrated by assuming the simplified geometry shown in Figure 12. All currents and voltages

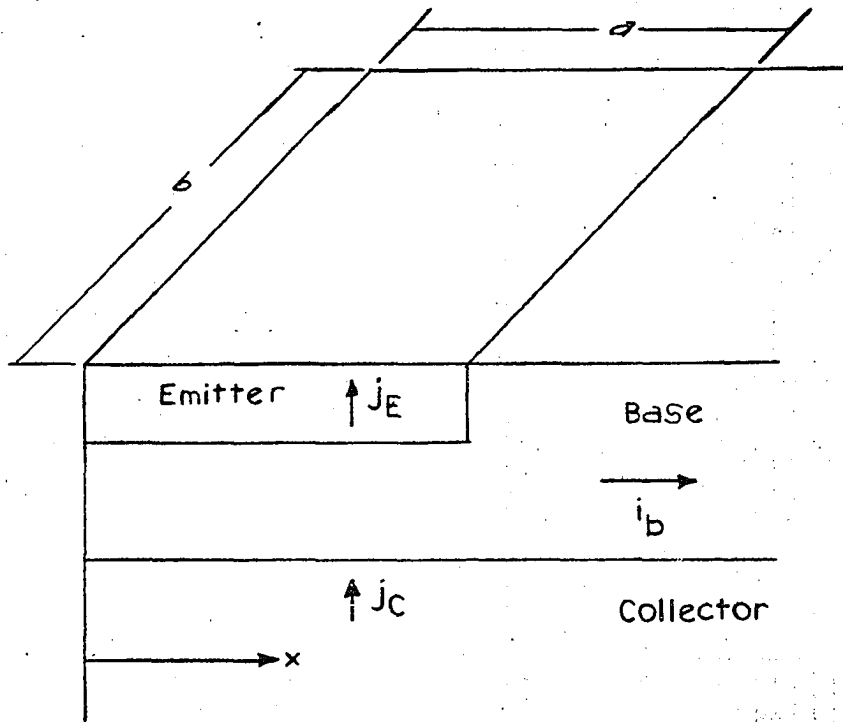


Figure 12. Simplified Transistor Geometry

are then uniform along the length of the emitter strip and only variations in the x direction need be considered. The emitter strip of the 2N709 is 13μ wide and 50μ long with a 13μ spacing between the emitter and the area where the evaporated contact to the base is made. The measurements of base spreading resistance for unit 12 correspond to a sheet resistance of the active base region in Figure 12 equal to 450 ohms.

The capacitive current from collector to base for unit 12 during turn-on with a 270 ohm load was previously found to be 16 ma. Of this 5 ma. shows up as an external base current, and the rest comprises a current from the active base region to the bulk base material. The emitter current density is proportional to $\exp(qv_b/kT)$ where v_b is the voltage at this point in the base, k is Boltzmann's constant, and T is the temperature, in degrees Kelvin. Since kT/q is about 26 mv. at room temperature reducing the forward bias on the emitter junction at any point by 60 mv. will reduce the emitter current density by a factor of 10. Assuming the geometry of Figure 12 with a base sheet resistance of 450 ohms the feedback current requires only about 0.5μ of lateral distance to change the base voltage by this much. By way of comparison the thickness of the base layer is slightly over 1μ . The area actually affected by the capacitive feedback current at any one time is thus much less than the total area of the emitter. Since the voltage gradient resulting from this current is so great it can exist only in the non-active regions of the base and will affect only the outer edge of the conduction region.

The negative feedback current must do two things in the process of reverse biasing a portion of the emitter. First it must remove the stored base charge represented by the σ_s of the area to be cut off. Since extending the area of the emitter which is cut off also requires that the portion which has previously been cut off have the junction voltage reduced still further, this latter process requires a charging current for the emitter transition capacitance. By neglecting the effect of the transition capacitance of the cut-off portion of the emitter and analyzing only the effect of the stored base charge, some useful generalizations can be drawn.

The emitter area in Figure 12 can be divided into two parts. For a distance, x , from the left hand side the emitter will be forward biased and unaffected by any transverse base currents, while the remainder of the emitter is cut off and not conducting. The effect of the collector to base capacitance will be a lateral base current, i_b , which biases the emitter into cutoff at the edge of the conducting region. The boundary of the conducting region will then retreat according to

$$\frac{dx}{dt} = - \frac{i_b}{b \sigma_s} \quad (52)$$

If i_c is the integral of j_c over the conducting area, the stored base charge per unit area will be

$$\sigma_s = \frac{i_c \tau_b}{M_n b x} \quad (53)$$

in which case

$$\frac{dx}{dt} = - \frac{i_b M_n x}{i_c \tau_b} \quad (54)$$

One of the more important results which can be obtained from Equation 54 is the reduction of the conducting area during the initial stages of turn-on. If the collector voltage is still nearly equal to V_{CC} so that nearly all of i_c serves to discharge the collector capacitance, the ratio of i_b to i_c is fixed by transistor and circuit capacitance. For unit 12 and the circuit used to obtain the photograph of Figure 11 this ratio is about 0.5. τ_b for a 2N709 can be obtained from data given for f_T and will average 0.24 ns. Then letting M_n be 5 and x be the full emitter strip width of 13 μ Equation 54 results in dx/dt being equal to - 130 μ /nsec. Midway through switching, i_b will be 11 ma. as measured, but the 270 ohm load will be drawing 22 ma. to make i_c equal to 38 ma. M_n will be equal to 2 at this point, and, letting x be 5 μ , dx/dt is - 12 μ /ns. More generally dx/dt is equal to - 10 x initially but reduces to - 2.4 x midway through switching.

This shows that the fastest reduction of conducting area occurs during the initial portion of the switching transient. This is also the point at which the emitter transition capacitance has the least effect, so allowance for this will only increase the difference between the rates. It follows that most of the pinch-in with its related increase in the base spreading resistance occurs very quickly, and almost all of the switching occurs with a reduced area.

Although it has little effect during the initial portion of the turn-on process, the value of the collector load resistance should influence the final magnitude of the pinch-in effect. Throughout most of the switching transient a lower value for the collector resistor will increase i_c in Equation 54 and thus reduce the pinch-in. This is borne out experimentally as can be seen by a comparison of Figures 10 and 11. With the higher load resistance a larger negative spike appears at the base, with no appreciable difference in the rate of change of the collector voltage.

A Model for Avalanche Switching

The model proposed for an avalanche transistor is shown in Figure 13. This is an extension of the model used by Hamilton et. al. (15) in a study of germanium alloy junction transistors. Modifications are necessary to allow for the effects of pinch-in and for the fairly different distribution of capacitance. The fact that a drift rather than diffusion mechanism is used for the transport of charge across the base does not fundamentally change the operation of the transistor. It does mean that τ_b is much smaller than would be the case for a uniform base transistor. Also the depletion region of the collector junction extends primarily into the collector rather than the base, thus the base thickness and τ_b are nearly independent of the collector voltage.

Many of the expressions needed for this model are counterparts of those derived in the last section. In terms of charge and current Equation 43 becomes

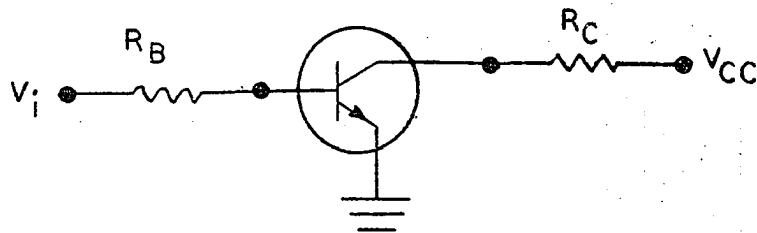
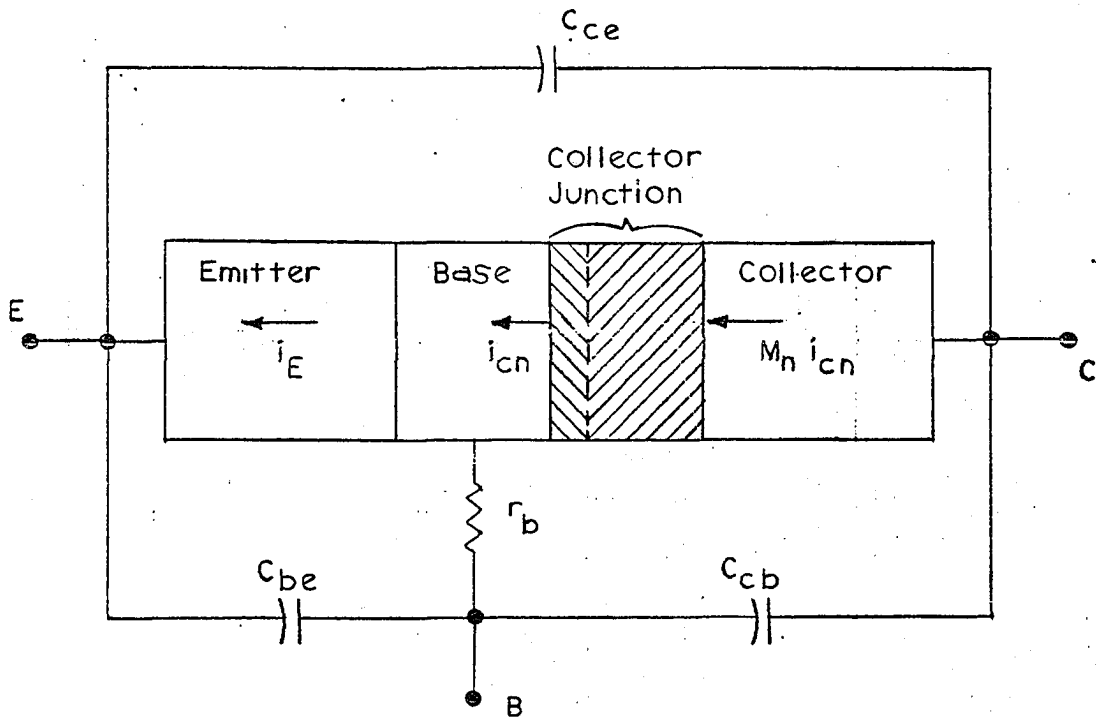


Figure 13. Model for Avalanche Transistor

$$q_s = \gamma\beta i_E \tau_b \quad (55)$$

for example. This combined with the counterpart of Equation 45 results in

$$i_{cn} = q_s / \tau_b \quad (56)$$

The total stored base charge changes according to

$$\frac{dq_s}{dt} = (M_n - 1/\gamma\beta) q_s / \tau_b - i_b \quad (57)$$

Since i_b is the current through the base spreading resistance this can be expressed in terms of the voltage of the base terminal and the forward voltage on the conducting portion of the emitter junction. In a silicon transistor only a small change in bias is required to greatly change the emitter current density once a significant current flow is present. Assume that the forward bias on the conducting portion of the emitter remains constant at some forward drop, V_F . Then

$$\frac{dq_s}{dt} = (M_n - 1/\gamma\beta) q_s / \tau_b + (v_B - V_F) / r_b \quad (58)$$

The base spreading resistance is not constant during switching, but, as has been shown, most of the pinch-in occurs early in the switching process, and, thus, the choice of a constant value is a good approximation. The capacitance, C_{ce} , consists of the internal capacitance from

collector to emitter. This can be extended to include capacitance to ground of the external collector circuit. The collector to base capacitance, C_{cb} , consists of the internal capacitance from collector to emitter. This can be extended to include capacitance to ground of the external collector circuit. The collector to base capacitance, C_{cb} , consists of stray capacitance and the collector transition capacitance. Because of the latter it is dependent upon the collector to base voltage. If, as is the case with the 2N709, the stray capacitance is the larger of the two this can be regarded as a constant with little error. There is very little stray capacitance from base to emitter, but since a portion of the emitter junction is cut-off during switching the transition capacitance of this portion of the emitter will provide a capacitance from base to emitter. This would more accurately be placed midway along r_b , but, in the interests of simplicity, it has been placed from the base terminal to the emitter terminal as C_{be} . All other parameters can either be directly measured or determined from observations of collector and base voltage during switching, but this one is more difficult. As switching proceeds the cut-off area of the emitter increases which tends to increase C_{be} . At the same time the reduction of the voltage on the rest of the emitter reduces the transition capacitance per unit area. For lack of any better method a constant value can be assumed and a reasonable guess made for it.

Result for a Resistance Load

Consider the case of avalanche turn-on with a collector load resistance of R_c , a collector supply voltage of V_{CC} , and an input trigger of V_i

coupled through an equivalent base circuit resistance of R_B . This is a simplified form of the circuit on which measurements were taken. One of the expressions which describe the action of this circuit has already been developed as Equation 58. A node voltage analysis at the collector terminal results in

$$(C_{cb} + C_{ce}) \frac{dv_C}{dt} + \frac{M_n q_s}{\tau_b} = (V_{CC} - v_C)/R_C + C_{cb} \frac{dv_B}{dt}. \quad (59)$$

Likewise

$$(C_{cb} + C_{be}) \frac{dv_B}{dt} = (V_i - V_F)/R_B - (v_B - V_F)(r_b + R_B)/r_b R_B + C_{cb} \frac{dv_C}{dt}. \quad (60)$$

These can be solved algebraically for dv_C/dt and dv_B/dt , and the result is

$$\frac{dv_C}{dt} = \frac{\left[(V_{CC} - v_C)/R_C - \frac{M_n q_s}{\tau_b} \right] (C_{cb} + C_{be})}{C_{cb} C_{ce} + C_{cb} C_{be} + C_{ce} C_{be}} + \frac{(V_i - V_F)/R_B - (v_B - V_F)(r_b + R_B)/R_B r_b}{C_{be} + C_{ce} + C_{ce} C_{be}/C_{cb}} \quad (61)$$

and

$$\frac{dv_B}{dt} = \frac{(V_i - V_F)}{R_B (C_{cb} + C_{be})} - \frac{(v_B - V_F) (r_b + R_B)}{R_B r_b (C_{cb} + C_{be})} + \frac{C_{cb}}{(C_{cb} + C_{be})} \frac{dv_C}{dt} \quad (62)$$

Equations 58, 61, and 62 provide a basis for finding the collector and base voltages during switching. Since M_n varies radically with the collector voltage this is a system of non-linear differential equations. Solution must be by numerical analysis. This is to be expected since Hamilton (16) used a much simpler model and still found it necessary to resort to numerical methods of solution. It is unlikely that there is any simpler method for a detailed analysis of avalanche switching.

As a check on the usefulness of this model a solution with circuit and transistor parameters corresponding to the circuit and transistor used in obtaining the waveforms of Figure 11 were used. Initial conditions were taken as $q_s = 0$, $v_B = V_F$ and $v_C = V_{CC}$. The collector voltage at each time was found by evaluating dv_C/dt and letting $v_C = \Delta t dv_C/dt$. The same approach was used for the other variables.

The process is not overly difficult to do by hand as fairly long time periods can be used during times of relatively linear change in the variables. If many solutions were desired a computer would naturally

be used.

The resulting solutions for v_B and v_C are shown in Figure 14. They follow the measured voltages quite well, and, considering the limitations of the sampling oscilloscope, no substantial difference can be noted. This verifies that the model used will provide useful predictions of the operation of a silicon planar transistor in the avalanche mode. Furthermore it shows that the phenomena which have been considered in detail individually will combine to produce the measured transients, and no further properties of the transistor are of great importance during switching.

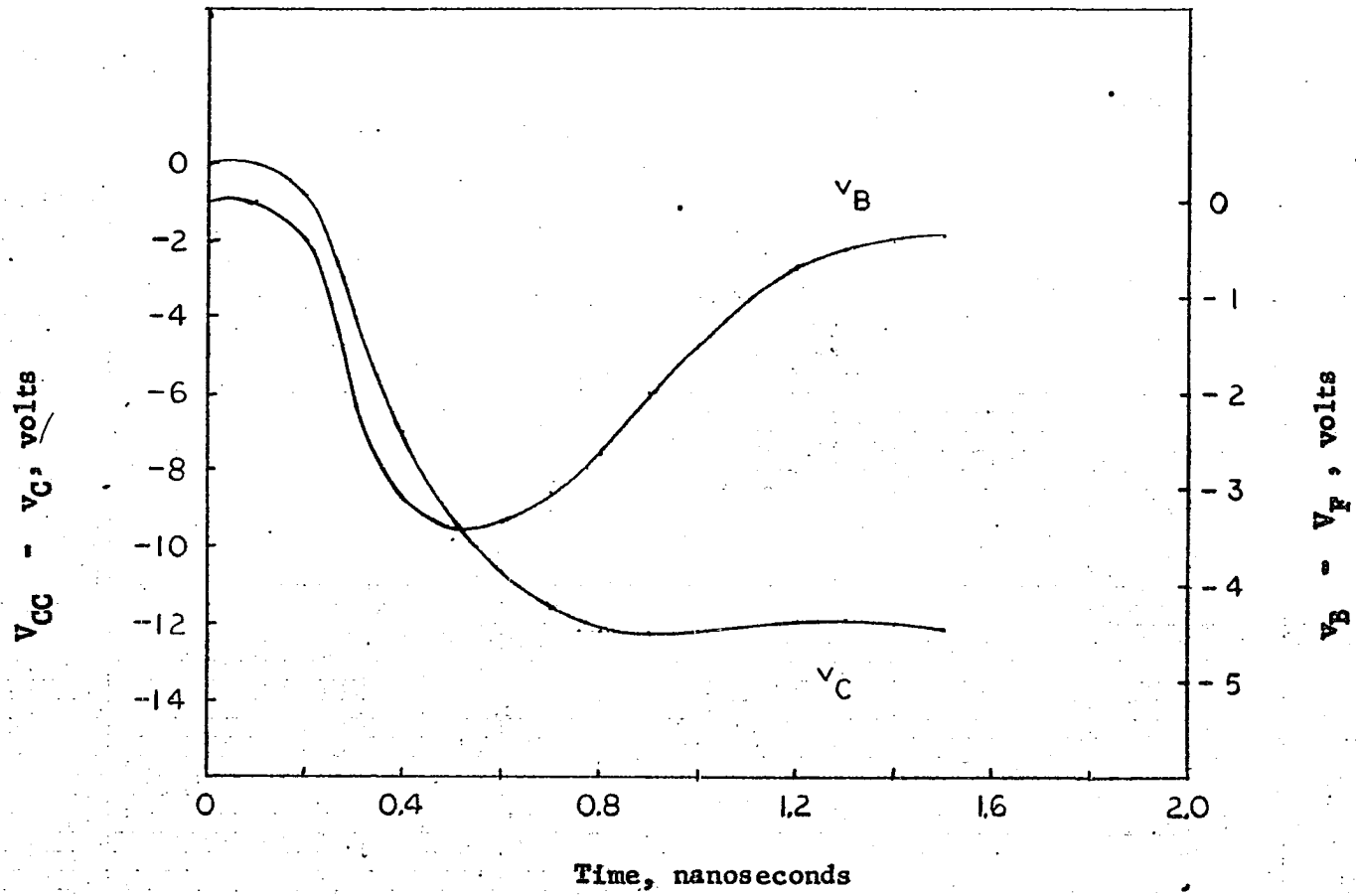


Figure 14. Calculated Voltages During Avalanche Transistor Turn-on

TURN-OFF CONTROL

Theory

General Methods of Turn-Off

Once the avalanche transistor is in the conducting state there are several ways it can be returned to the non-conducting state. If the turn-on drive is removed and the collector temporarily held at some voltage below the equilibrium voltage, $V_{CE(on)}$, the normal reverse base current will reverse bias the emitter so that, when the collector voltage is permitted to rise, the transistor will remain in the non-conducting state. Since a small reverse base current is required to minimize $V_{CE(on)}$ a fairly long time is required to remove the stored base charge and reverse bias the emitter. Also after the transistor is turned off the collector voltage can not be returned to V_{CC} too rapidly or else the collector voltage change coupled through C_{cb} will overcome the reverse bias and turn the transistor on again.

The method suggested by Figure 1 is to temporarily increase the reverse base bias so that the only stable condition is the non-conducting state. This will work and will be considered in more detail later. There are several difficulties which occur, especially at higher current levels, but the speed possible with this method makes it very attractive.

Another possible method of turn-off is to temporarily change the collector load line, either by reducing V_{CC} or increasing R_C , so that with even normal reverse base bias the only stable state is the off state. This was used in the turn-on test circuit of Figure 9 where a

long recovery time was not troublesome. Once the 120 pf. capacitor discharges the transistor effectively has a 10 K. load resistance and is turned off by the reverse base bias. The long charging time for the 120 pf. capacitor prevents C_{cb} from providing enough current to the base to overcome the reverse bias.

Base Control

During avalanche turn-on positive feedback is provided by the avalanche multiplication of the collector junction. At the same time the collector to base capacitance provides a negative feedback. Since the capacitive feedback depends upon the rate of change of the collector voltage it opposes any attempt to turn the transistor off in the same manner that it opposed the turn-on process. Since collector avalanche depends upon the collector voltage and is independent of the rate of change of this voltage the effect of avalanche will still be to try to turn the transistor on, and thus this effect must also be overcome during turn-off.

One item of interest is the critical base current necessary to just overcome avalanche multiplication and leave only one stable state for the transistor. This would be the base current for which the collector characteristic is just tangent to the collector load line as represented by the $I_B = -4I$ curve in Figure 1. In Equation 6 the departure of $\gamma\beta$ from 1 is important only at voltages near $V_{(BR)CEO}$. If $\gamma\beta$ is 1 and M_n is described by Equation 38

$$I_C = - \frac{V_B - V_o}{V_C - V_o} I_B \quad (63)$$

Since I_C is equal to $(V_{CC} - V_C)/R_C$ the base current corresponding to each collector voltage is

$$I_B = - \frac{(V_{CC} - V_C)(V_C - V_0)}{R_C (V_B - V_0)} \quad (64)$$

The critical tangency occurs at the maximum magnitude of I_B and is

$$I_{B(\text{crit})} = - \frac{(V_{CC} - V_0)^2}{4 R_C (V_B - V_0)} \quad (65)$$

The collector voltage while the transistor is in the conducting state is generally somewhere around V_0 , so a reasonably accurate alternative to Equation 65 is

$$I_{B(\text{crit})} = - \frac{(V_{CC} - V_0)}{4(V_B - V_0)} I_{C(\text{on})} \quad (66)$$

The current gain possible for base turn-off in avalanche mode operation is then somewhat better than 4.

Problems of Base Control

So long as only a small change in base voltage is needed to turn the transistor off there is still only a small amount of power required for switching control as compared to the power being controlled. This is then still a very practical method of controlling the state of the transistor. In the study of the turn-on transients of an avalanche

transistor it developed that a large transverse base current attempting to reverse bias the emitter affected only the periphery of the conducting region and led to a pinch-in effect. This effect can also be produced by the currents applied to turn-off the transistor. While pinch in during turn-on had no harmful effect, other than requiring a derating of the maximum power dissipation specification, the effects which occur during turn-off are more serious. First, pinch-in increases the base resistance. The turn-off current must be withdrawn through this resistance, and thus more power is required to turn the transistor off. A second, and more serious, problem is the possibility of triggering secondary breakdown of the collector junction.

A crucial factor in determining the pinch-in effect is the magnitude of the lateral base current. Again assuming the simplified geometry of Figure 12 let Δx be the distance required for a lateral current of i_b to produce a 60 mv. change in the base potential. Then

$$\Delta x = \frac{60 \text{ mv.}}{i_b R_s} b \quad . \quad (67)$$

A comparison of Δx with the width of the emitter strip will provide a measure of the amount of pinch-in possible. If Δx is much smaller than the emitter width only the periphery of the conducting region will be affected by the turn-off current, and turn-off can proceed only by crowding the current into an ever smaller area. A larger value for Δx indicates that a large portion of the conducting portion of the emitter is being reverse biased simultaneously. With b equal to 50 μ

and an R_s of 450 ohms a turn-off current of 1 ma. results in a Δx of 6.7 μ . Compared to a strip width of 13 μ this would indicate that, at worst, half of the emitter is made inactive. Since the collector current decreases during turn-off the actual current density probably remains about the same, and there should be no real problem at this current or lower currents. Since this turn-off current will control about 5 ma., pinch-in should be no problem for collector currents below 5 ma., but it will become increasingly significant at collector currents above 10 ma.

Suppose that a transistor operating in the avalanche mode has a large enough reverse bias applied to make Δx much smaller than the emitter dimensions, but not adequate to switch the transistor to the non-conducting state. Then the collector voltage will increase, and avalanche multiplication will increase the current density of the conducting area. Although the geometry may differ from that used in the development of Equation 54 the conducting area will continue to diminish in some similar manner. The pinch-in effect will end only when some area with dimensions comparable to the dimensions of Δx is reached. Secondary breakdown of a junction is thermally triggered and results in a part of the collector junction becoming molten. (18). This is obviously not good for the junction and will eventually destroy it. If the power dissipation in the remaining area is large and the area has been seriously constricted it is very likely that a high enough temperature will be generated to cause secondary breakdown.

Any signal which turns a transistor off must draw sufficient base

current to remove the stored base charge, q_s , to cut off the emitter by partially discharging the emitter transition capacitance, and to overcome the negative feedback from the collector to base capacitance. This must be done in normal mode operation as well as in avalanche mode operation. If the transistor is to be switched off through the avalanche region an additional reverse base current is required to overcome the collector hole current which results from avalanche multiplication.

The total charge which must be removed from the transistor during the turn-off process is

$$q_{B(\text{off})} = q_{s(\text{on})} - C_{TE} \Delta v_{b(\text{av.})} + C_{cb} (\Delta v_C - \Delta v_B) + \int (M_n - 1) q_s dt / \tau_b . \quad (68)$$

Here $\Delta v_{b(\text{av.})}$ is the average change in the potential of the base layer after the emitter is reverse biased and will be a negative quantity.

The effects of emitter efficiency and base recombination have been neglected in this expression and are seldom of importance.

Were it possible to reverse bias the emitter instantaneously the collector voltage during turn-off would be determined by the time constant of the collector circuit. This time constant then provides a lower limit on the turn-off time which can be obtained. For any given transistor it can be reduced only by reducing the collector load resistance. This in turn involves higher collector currents, greater turn-off

currents, and the problems related to pinch-in.

The last term of Equation 68 is the term which allows for the effect of avalanche multiplication on turn-off. Initially M_n is essentially 1, and q_s is equal to $q_{s(on)}$. As turn-off proceeds M_n will increase and q_s decrease. If q_s can be reduced to 0 while the $M_n - 1$ term is still small there is very little effect from this term. Without the effect of multiplication the current density of the conducting area does not increase, and eventually the entire emitter junction can be reverse biased without concern about hot spots.

If the stored base charge is removed before the collector voltage has risen to a point at which avalanche multiplication becomes significant, switching should be similar to that which occurs in normal mode operation. Also the turn-off time will approach the limitation imposed by the collector time constant. An idea of the current required for such switching can be obtained by assuming that the base current will remove the entire amount of stored base charge in a time equal to the collector time constant $R_C (C_{cb} + C_{ce})$. If the effects of avalanche multiplication and the emitter transition capacitance are neglected, and if the effect of C_{cb} is included by assuming that on the average half of the initial collector current contributes to the charging of the collector capacitance during this period, the end result is that for fast switching

$$i_B = - \frac{(I_{C(on)})^2 \tau_b}{(C_{cb} C_{ce}) \Delta v_C} - \frac{1}{2} \frac{C_{cb}}{C_{cb} C_{ce}} I_{C(on)} \quad (68)$$

Even if the effects of avalanche are minimized by fast switching, the control current required increases more than linearly with the current being controlled, and the question arises as to how much control power one is willing to use to achieve rapid turn-off.

Measurements

Test Circuit

In order to measure waveforms during turn-off it is necessary to first turn the transistor on and then apply the turn-off signal at some later time. This can be done with two pulses of course, but a simpler approach is to just apply a constant reverse bias adequate to turn the transistor off, and merely use the incoming pulse to overcome it momentarily. At the end of the input pulse the reverse bias is again applied to the base and measurements of base, and collector waveforms during turn-off are made at this time. The circuit used is shown in Figure 15. It is similar to that used for turn-on. The only changes are a smaller resistor from the pulse input line to the base, and the larger coupling capacitor on the output.

The effective voltage of the turn-off bias source can be measured by measuring the d.c. voltage at the base terminal with the transistor removed. This voltage applied through the base circuit impedance of 200 ohms is the bias acting to turn the transistor off. The effective collector supply voltage is the voltage across the 750 pf. coupling capacitor during turn-off. This can be determined by measuring the voltage across this capacitor with the transistor in the circuit and

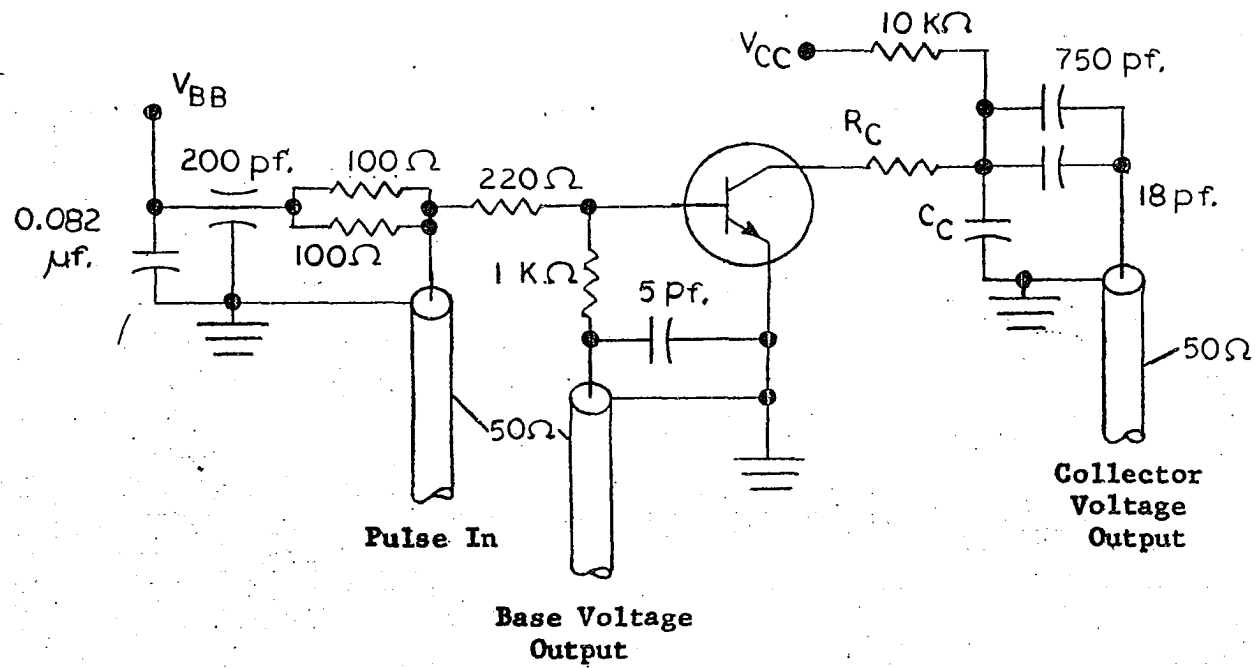


Figure 15. Circuit for Measuring Turn-Off

then correcting for the small amount it will discharge while the transistor is conducting.

Results

The required amount of turn-off bias is measured as follows. With V_{CC} set at some desired value V_{BB} is adjusted so that the transistor just turns off. The pulse generator is adjusted to provide an input pulse equal to the magnitude of V_{BB} plus 1 volt, and V_{BB} is adjusted again if necessary. There is a coupling between the bias setting and pulse amplitude which reduces the interdependence of these settings, and there is no problem in obtaining a balance. From the collector waveform, measurements of the collector current being switched and the turn-off time are made. The base voltage and current are not constant during turn-off, so only a measurement of the base voltage immediately upon application of the turn-off bias is made. From this the base current which exists at this time can be found.

Table 5 shows these measurements as well as the calculated value for $I_{B(crit)}$ and the base current of Equation 68. With minimum turn-off bias and the 1050 ohm load turn-off times of 9 or 10 nsec. were measured as compared to a limit of around 6 nsec. imposed by the collector time constant. The one exception was unit 13 with a 50 volt collector supply voltage where the relatively low supply voltage permitted a 14 nsec. turn-off. These were maximum turn-off times as more turn-off power reduced the times and less resulted in the transistor failing to turn-off. A similar situation existed with unit 12 and the 270 ohm load where the maximum turn-off time was 4 nsec. Unit 2 with its smaller

Table 5. Turn-off Bias for Avalanche Transistors

Unit	$V_{(BR)CBO}$ volts	Collector Load, ohms	V_{CC} volts	$I_{C(ON)}$ ma.	$V_{(off)}^a$ volts	$i_{B(in)}^b$ ma.	$I_{B(crit)}$ ma.	$I_{B(off)}^c$ ma.
12	23	1050	18.6	12	-0.40	5.3	1.7	4.8
		1050	20.4	14	-0.97	7.1	2.5	5.4
		270	16.4	33	-3.55	17	4.2	21
2	26	1050	20.0	11	-0.40	4.6	1.6	4.4
		1050	23.8	15	-0.88	7.0	2.9	5.6
		270	23.4	48	-3.05	15	10.6	30
6	32	1050	24.0	16	-0.78	6.5	1.9	6.2
		1050	26.1	21	-1.54	9.7	2.6	8.3
7	39	1050	30.1	18	-1.02	7.1	1.8	6.7
		1050	34.6	23	-1.7	10.2	3.4	8.6
10	51	1050	43	31	-1.17	8.9	4.5	11.4
		1050	47	33	-1.8	10.4	6.1	12.2
13	65	1050	50	32	-0.68	7.0	3.2	11.4
		1050	60	40	-1.81	11.5	6.7	14.8

^aMost positive value of base bias which will turn the transistor off.

^bInitial base current during turn-off.

^cReverse base current for fast turn-off calculated from Equation 68.

base resistance had a slower time of 9 nsec. with minimum turn-off bias.

Neither of the calculated base currents is intended as a prediction of the measured turn-off bias. They do, however, aid the interpretation of the measured results. Note the strong relationship between the initial base current during turn-off and the base current for fast turn-off predicted by Equation 68. This indicates that, for the 200 ohm base source resistance of the test circuit, less reverse bias voltage is required to quickly remove the stored base charge than to draw a smaller base current through the increase base spreading resistance after pinch-in has occurred.

Methods of Reducing Required Turn-Off Bias

As has been noted the effects of avalanche multiplication during turn-off are minimized if the stored base charge can be removed before the collector voltage reaches the region of high multiplication. This can be accomplished by providing an initial reverse base current similar to that predicted by Equation 68. The placement of a capacitor across the 220 ohm resistor to the base of the transistor will increase the initial base current and should permit a reduced setting for the turn-off bias. This proves to be the case. Unit 12 with a 270 ohm load and an equivalent collector supply voltage of 16.4 volts required a turn-off bias of -3.55 volts. An 18 pf. capacitor placed in parallel with the 220 ohm resistor reduces the required bias to -1.65 volts, and the turn-off time with minimum bias is reduced from 4 ns. to 2 ns. despite an increase of the collector supply voltage to 17.4 volts.

The reverse base current for fast switching as predicted by Equation 68 is reduced if C_{ce} is increased. This increases the time constant of the collector circuit and allows more time to remove stored base charge. This can easily be done by adding capacitance from collector to ground. The addition of 5 pf. to the collector of the transistor in the circuit just considered and still using unit 12 permitted the use of a collector supply voltage of 19.4 volts. At the same time that the collector supply voltage is increased the required base bias for turn-off is reduced to 1.0 volts. The turn-off time is slower of course, and is 4.4 ns. Increasing the capacitance from collector to ground is a simple way of reducing the required turn-off bias at the cost of a slower turn-off time and greater overshoot during turn-on.

There is another method by which small reductions in the required turn-off bias may be made. If positive drive is provided before turn-off so that the transistor has actually been driven into the normal region of operation, a greater rise in the collector voltage is required before avalanche becomes significant. This increases the time available to remove the stored base charge, but also increases the base charge. The net effect is to reduce the reverse drive required by a small amount.

Applications of Base Turn-Off Control

While base control for turn-off affords the possibility of quite fast turn-off times, at the low collector impedance levels required to obtain these speeds considerable control current is generally required.

It still seems likely that there are times when the difficulties of base control are worth the high speed and relatively simple turn-off circuitry required. One interesting possibility is to use some of the output signal from the collector and return it to the base at some later time as a turn-off signal. The avalanche transistor would then be generating its own turn-off signal, and no power from an external source need be provided for this purpose.

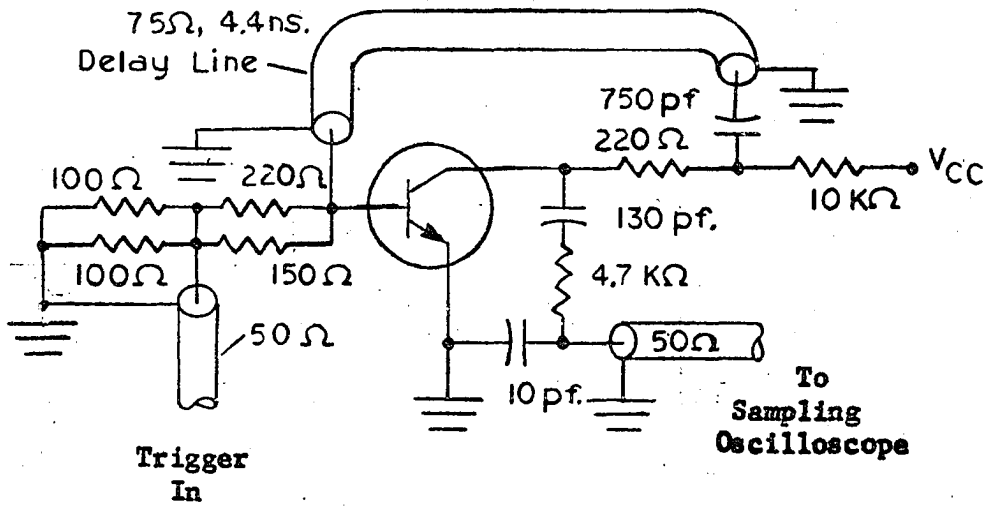
An Astable Avalanche Transistor Circuit

In a pulse application this could easily be done by feeding a part of the output pulse to the base through a delay line. A circuit which does this is shown in Figure 16a. A 75 ohm delay line is placed in series with the 220 ohm load. Of the total negative pulse appearing at the collector 75% appears across the load and 25% is delayed by 4.4 nsec. and returned to the base as turn-off control. The waveform measured with this circuit is shown in Figure 17^a. This circuit provides a turn-on time of 1 nsec. and a turn-off time of 2 nsec.

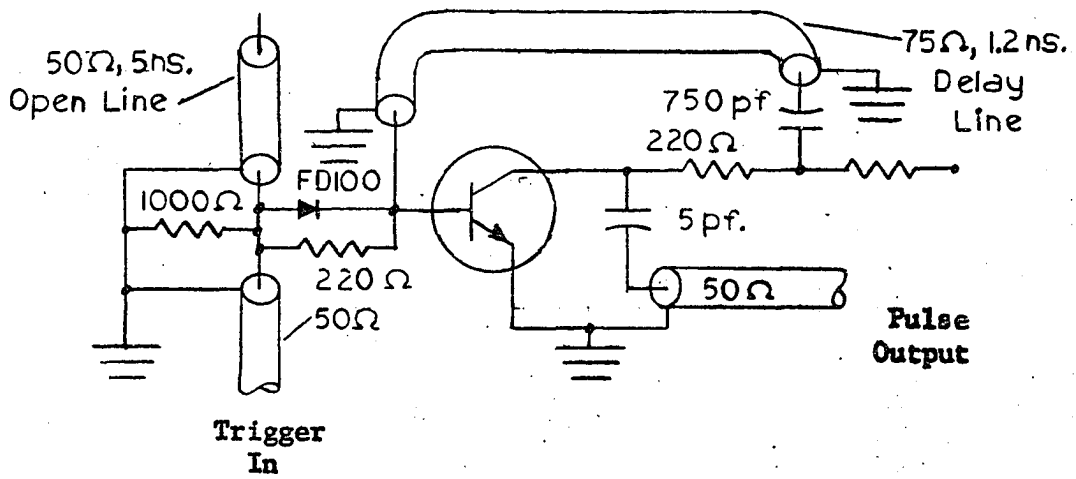
Of the total pulse appearing at the collector about 10 volts will be across the 220 ohm load and the remaining 3.3 volts appear across the 75 ohm coaxial delay line. This much of the output pulse then serves to turn the transistor off. In particular when one considers the voltage being switched these are very fast switching times, and a reasonable pulse shape is maintained.

A Fast Rise, Quick Recovery Pulse Generator

One of the more commonly used avalanche transistor circuits is the pulse generator of Figure 7b. This circuit can easily be adapted



a. An Astable Avalanche Circuit



b. A Fast Rise, Quick Recovery, Pulse Generator

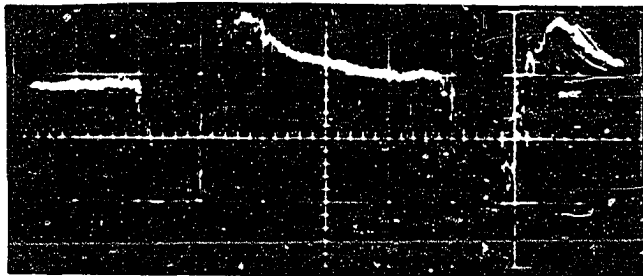
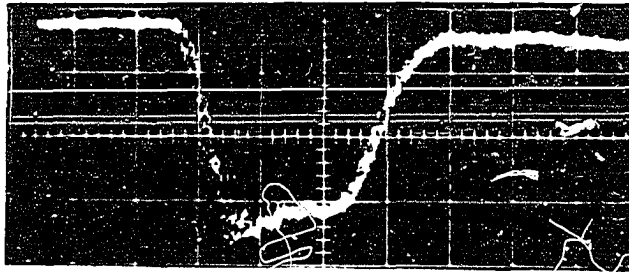
Figure 16. Applications of Base Turn-Off Control

Figure 17a. Collector Waveform of Astable Avalanche
Transistor Circuit

The transistor is unit 2 of the 2N709's with a
24 volt collector supply. The vertical scale is
4.5 volts/cm. and the time scale is 2 nsec./cm.

Figure 17b. Output of Fast Rise, Quick Recovery, Pulse
Generator

The transistor is unit 2 of the 2N709's with a
24 volt collector supply. The vertical scale is
1 volt/cm. and the time scale is 2 nsec./cm.



to a triggered operation and is used when pulses with very fast rise times are needed. The recovery time is limited by the time required to recharge the capacitor, C , and the internal collector capacitance of the transistor. This time can be reduced by reducing R_C , but more reverse base bias is then required to turn the transistor off after each pulse. This, in turn, leads to triggering difficulties.

The recovery problem can be solved by the use of delayed coupling of the output voltage back to the base to provide turn-off bias only when needed. Such a circuit is shown in Figure 16 b. In this circuit a 5 pf. capacitor is discharged through a 50 ohm output line to provide the desired pulse. At the same time a turn-off pulse is generated and returned to the base as in the previous circuit.

Two triggering pulses in rapid succession are required if the recovery time is to be tested. This is accomplished by reflecting the original trigger pulse from the end of an open line. The resulting output pulses are shown in Figure 17b. The 10 ns. recovery time is required if full trigger sensitivity is to be maintained, but it can be triggered even sooner if additional trigger power is available. The rise time of the output pulses cannot be determined as that measured is simply the rise time of the sampling oscilloscope. The lower collector load resistance may somewhat reduce the rise time possible with such a circuit, but this still is much better than could be hoped for in normal mode operation. The recovery time is limited by the time required for the voltage on the delay line to return to normal. Better termination of this line and probably a more careful choice of the line length should permit even further reductions of recovery time.

SUMMARY AND CONCLUSIONS

Findings

In the course of this study of the avalanche mode operation of transistors some important new results emerged. They are the constriction of the current carrying area of the transistor during avalanche switching. The development of a model which allows for this effect, and a determination of the role of the collector junction construction and breakdown voltage upon the transistor characteristics.

Measurements of collector and base voltages during avalanche switching resulted in waveforms which could not be explained by previous theories of avalanche switching. These measurements showed that part of the emitter was being reverse biased during switching, and that the constriction of the current carrying area led to an increased base spreading resistance.

The cause of this pinch-in effect is a transverse current in the base region which attempts to reverse bias the emitter junction. During turn-on the collector to base capacitance and the rapid change in collector voltage combine to provide a sizable negative feedback into the base. The collector capacitance of a transistor was found to be distributed so that this feedback resulted in transverse base currents and thus a pinch-in effect. A double diffused structure emphasizes this effect because the collector junction area is considerably greater than the emitter junction area. A turn-off current applied to the base of the transistor can also cause a severe constriction of the conducting area, and this was found to be the major problem involved in base control.

A simplified geometry was assumed for the transistor to show how a transverse base current causes this pinch-in. It was shown that at the levels of transverse current generally encountered in avalanche switching only the outer edge of the conducting area is affected by this current. During switching the boundary of the conducting area is continually forced to retreat, and the total amount of pinch-in depends, among other things, upon the time required for switching.

Previous models for avalanche transistors assumed a uniform base potential. Such a model proved to be unsatisfactory for the transistors used in this study. A new model was developed which includes the effect of pinch-in and capacitance distribution found in a double diffused transistor. This model proved to be capable of predicting the wave-forms which resulted during the turn-on of an avalanche transistor.

A theoretical study of the avalanche multiplication of step and graded junctions of various breakdown voltages was made. The objective was to find how as much avalanche multiplication as possible over as wide a range of the collector voltage as possible could be obtained. It was shown that a step junction is preferable to a graded junction, but that junctions similar to step junctions can be made by diffusion, and these are satisfactory for avalanche operation. Also a relatively low breakdown voltage is preferred with the optimum value being around 15 volts.

The threshold effect in avalanche multiplication rather than internal field emission was shown to be the primary limiting factor in

any attempt to design an avalanche transistor to operate even lower voltages.

Design of an Avalanche Transistor

These findings are applicable to any attempt to select or build a transistor for avalanche mode operation. Apart from collector construction and breakdown voltage there are several other characteristics desirable in such a transistor. In order to minimize the pinch-in effect the collector to base capacitance and base resistivity should be kept as low as possible. From the standpoint of base resistivity something other than an NPN silicon transistor would be preferable, but a heavily doped base will minimize this problem without compromising upon the desired avalanche multiplication.

The base transit time should be as small as possible since this will permit faster operation and reduce the charge which must be removed during turn-off. This can be accomplished by a thin, heavily graded, base as is used in very high frequency transistors anyway. This incidently tends to result in a heavily doped base and is compatible with the desire for very sharply diffused collector junctions of low breakdown voltages. In general, attempts to obtain one of the parameters desired for an avalanche transistor aid rather than interfere with attempts to obtain other desired parameters.

Areas for Future Study

It would be of interest to build some avalanche transistors with breakdown voltages in the 10 to 20 volt range and see what results can

be obtained with them. Considering the transistors now being built for normal operation these should not be so different as to involve any new problems in construction. There may also be changes that can be made in the geometry of a transistor which will reduce the pinch-in problem. Maybe one of the other common geometries and perhaps a narrower emitter, if possible, would improve operation. Although the desirable characteristics are now known there is more to be done in determining methods of building the transistor to optimize total operation.

It may be that transistor failures as a result of secondary breakdown are, in part, the result of pinch-in during avalanche switching. A careful study of thermal effects and the role of junction irregularities is needed to determine this. If such is the case it may suggest methods of circuit or transistor design which will reduce the likelihood of this failure mode. In practice many circuits using NPN silicon transistors are operated, in part, in the avalanche mode. This is done to utilize a greater portion of the collector voltage range, and the different properties of the transistor in the avalanche region are not desired or even considered. Treating such operation as avalanche mode operation could result in lower failure rates.

Finally the speed obtained with base turn-off control suggests that there are more applications for avalanche transistors than have been used up to now. The two circuits shown in the previous chapter are examples. Even these were put together rather quickly and probably do not represent the full potential of these circuits. One intriguing possibility is an application as a class C amplifier. This involves

switching operation of the transistor and should utilize the full collector voltage range rather than just a small part of it.

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